Papers Published

1. Minah Lee, Jinwoo Kim, Arvind Singh, Hakki Mert Torun, Madhavan Swaminathan, Sung Kyu Lim, and Saibal Mukhopadhyay, " On the Design of Energy-Efficient I/O Circuits for Interposer-based 2.5D System-in-Package," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, 2018.
2. Minah Lee, Arvind Singh, Hakki Mert Torun, Jinwoo Kim, Sung Kyu Lim, Madhavan Swaminathan, and Saibal Mukhopadhyay, "Automated Generation of All-Digital IO Library Cells for System-in-Package Integration of Multiple Dies," IEEE Electrical Performance of Electronic Packaging and Systems, 2018.
3. H. M. Torun, M. Larbi and M. Swaminathan, "A Bayesian Framework for Optimizing Interconnects in High-Speed Channels," 2018 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO), Reykjavik, 2018.
4. H. M. Torun and M. Swaminathan, "High-Dimensional Global Optimization Method for High-Frequency Electronic Design," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 6, pp. 2128-2142, June 2019.
5. Minah Lee, Arvind Singh, Hakki Mert Torun, Jinwoo Kim, Sung Kyu Lim, Madhavan Swaminathan, and Saibal Mukhopadhyay, "Automated Generation of All-Digital I/O Library Cells for Multiple Dies in System-in-Package Integration," Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.
6. Hakki Torun, Nihar Dasari, Arvind Singh, Minah Lee, Jinwoo Kim. Heechun Park, Hyouk Joon Kwon, Eric Qin, Tushar Krishna, Sung Kyu Lim, Saibal Mukhopadhyay, and Madhavan Swaminathan, "Design Space Exploration of Power Delivery in Heterogeneous Integration," Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.
7. Jinwoo Kim, Eric Qin, Heechun Park, Tushar Krishna, and Sung Kyu Lim, "Enabling Heterogeneous IP Reuse with Interposer-based 2.5D ICs and Custom Interface Protocol," Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.
8. Jinwoo Kim, Gauthaman Murali, Heechun Park, Eric Qin, Hyoukjun Kwon, Venkata Chaitanya Krishna Chekuri, Nihar Dasari, Arvind Singh, Minah Lee, Hakki Mert Torun, Kallol Roy, Madhavan Swaminathan, Saibal Mukhopadhyay, Tushar Krishna and Sung Kyu Lim, "Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse," ACM Design Automation Conference, 2019.
9. V. C. K. Chekuri, N. Dasari, A. Singh and S. Mukhopadhyay, "Automatic GDSII Generator for On-Chip Voltage Regulator for Easy Integration in Digital SoCs," 2019 IEEE/ACM International Symposium on Low Power Electronics and Design, 2019.
10. Hakki Torun, Huan Yu, Nihar Dasari, Venkata Chaitanya Krishna Chekuri, Arvind Singh, Jinwoo Kim, Sung Kyu Lim, Saibal Mukhopadhyay and Madhavan Swaminathan, "A Spectral Convolutional Net for Co-Optimization of Integrated Voltage Regulators and Embedded Inductors," IEEE International Conference on Computer-Aided Design, 2019.
11. V. C. K. Chekuri, N. R. Rahman, A. Singh, N. Dasari, E. Lee and S. Mukhopadhyay, “Automatic GDSII Generator for On-Chip Voltage Regulator for Easy Integration in Digital SoCs”, Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2020.
12. Minah Lee, Arvind Singh, Hakki M.Torun, Jinwoo Kim, Sung Kyu Lim, Madhavan Swaminathan, and Saibal Mukhopadhyay, "Automated I/O Library Generation for Interposer-based System-in-Package Integration of Multiple Heterogeneous Dies," IEEE Transactions on Components, Packaging, and Manufacturing Technology. Vol. 10, No. 1, pp. 111-122, 2020.

13. V. C. K. Chekuri, N. M. Rahman, E. Lee, A. Signh and S. Mukhopadhyay, "A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process," 2020 IEEE Custom Integrated Circuits Conference, 2020.
14. Majid Ahadi Dolatsara, Madhavan Swaminathan, “Determining worst-case eye height in low BER channels using Bayesian optimization,” 2020 IEEE 11th Latin American Symposium on Circuits & Systems, 2020.

Papers Under Review (as of July 2020)

15. Majid Ahadi Dolatsara, Jose Hejase, Wiren Dale Becker, Jinwoo Kim, Sung Kyu Lim, and Madhavan Swaminathan, “Worst-case Eye Analysis of High-speed Channels Based on Bayesian Optimization,” IEEE Transactions on Electromagnetic Compatibility.
16. Gauthaman Murali, Heechun Park, Eric Qin, Hakki Mert Torun, Majid Ahadi Dolatsara, Madhavan Swaminathan, Tushar Krishna, and Sung Kyu Lim, “Clock Delivery Network Design and Analysis for Interposer-based 2.5D Heterogeneous Systems,” IEEE Transactions on Very Large Scale Integration Systems.
17. Jinwoo Kim, Venkata Chaitanya Krishna Chekuri, Nael Mizanur Rahman, Majid Ahadi Dolatsara, Hakki Torun, Madhavan Swaminathan, Saibal Mukhopadhyay and Sung Kyu Lim, “Chiplet/Interposer Co-Design for PPA vs. Power Integrity Tradeoffs in Heterogeneous 2.5D ICs”, IEEE International Conference on Computer-Aided Design.
18. Jinwoo Kim, Gauthaman Murali, Heechun Park, Eric Qin, Hyoukjun Kwon, Venkata Chaitanya Krishna Chekuri, Nihar Dasari, Arvind Singh, Minah Lee, Hakki Mert Torun, Kallol Roy, Madhavan Swaminathan, Saibal Mukhopadhyay, Tushar Krishna and Sung Kyu Lim, “Architecture, Chip, and Package Co-design Flow for Interposer-based 2.5D Chiplet Integration Enabling Heterogeneous IP Reuse,” IEEE Transactions on Very Large Scale Integration Systems.
19. Jinwoo Kim, Venkata Chaitanya Krishna Chekuri, Nael Mizanur Rahman, Majid Ahadi Dolatsara, Hakki Mert Torun, Madhavan Swaminathan, Saibal Mukhopadhyay and Sung Kyu Lim, “Silicon vs. Organic Interposer: PPA and Reliability Tradeoffs in Heterogeneous 2.5D Chiplet Integration,” IEEE International Conference on Computer Design.