VENKATESH AVULA
251 10th Street NW, Apt. C401, Atlanta, GA 30318, USA
+1 208 874 9137
venkatesh.avula@ieee.org

EDUCATION

PhD in Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA 2018-current
Research focus: Power and thermal integrity of heterogeneously integrated voltage regulator architectures.
MS in Electrical Engineering, University of Idaho, Moscow, USA 2015-2016
Thesis: Novel Methods and Algorithms for Fitting and Equivalent Circuit Synthesis of Multi-port Systems' Frequency Response for Time-domain Simulation
B.Tech in Electronics and Communication Engineering, Cochin University of Science and Technology, India 2000-2004

PROFESSIONAL EXPERIENCE

Micron Boise, USA 2016-2018
Package signal and power integrity engineer, participated in the DDR5 package electrical specification development.

Seagate (formerly LSI / Avago Technologies) Bangalore, India 2013-2015
Signal and Power Integrity engineer, responsible for co-design, simulation, electrical analysis and characterization of IO interfaces- PCIe, SAS and DDR for datacenter flash storage products including PCB, package and silicon ICs.

Tektronix Bangalore, India 2008-2013
Lead Engineer, developed signal integrity test solutions for characterization of Physical layer of high-speed serial communication standards.

PUBLICATIONS

Journals-

• Venkatesh and Ata,"Parallel, optimized, error-maximama agnostic Pole Residue Equivalent System Solver", IEEE CPMT journal, 2017
• Venkatesh and Ata, "A Novel Iterative Algorithm for Approximating Equivalent Circuits of Numerical Transfer Functions", Wiley International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, 2016

Conferences-

• N Yamin, V Avula, A Zadehgol, A novel method for identifying complex zeros by searching the laplace-plane for local minima, 2017 International Workshop on Antenna Technology
• Venkatesh and Ata, "Coarse-to-fine Malleable Pole/Residue Equivalent System Solver", IEEE EDAPS 2016 , USA
• Venkatesh and Ata, "A Novel Method for Equivalent Circuit Synthesis from Frequency Response of Multi-port Networks", IEEE EMC Europe conference 2016, Poland
• Venkatesh and Ata, "A Novel Iterative Method for Approximating Frequency Response with Equivalent Pole/Residues", IEEE EMC SI/PI Conference 2016, Canada
• Venkatesh and Ata, "Pole Residue Equivalent System Solver", IEEE Signal Power Integrity 2016, Italy
• Venkatesh and Steve Sandler, "Evaluation of Gallium Nitride MOSFET for VRM Designs", DesignCon 2016, USA
• Venkatesh, "Novel Stressed Eye Tolerance Test Methodology using IBIS AMI Modeling", DesignCon 2015, USA
• Venkatesh, "Model based Link Budget Analysis considering Signal and PDN Interactions", DesignCon2014, USA
• Alfred, Venkatesh et al, "IBIS AMI Modeling of Retimer & Analysis of Active Serial Links", DesignCon2014, USA
• Venkatesh and Wessling, "Physical Layer Characterization Challenges in MOST", MOST Forum 2013, Germany
• Mythili and Venkatesh, "Precision Array Beam steering using Fractional Delay Filters", SYMPOL 2003, India

AWARDS

- Outstanding Master's Student Research and Creative Activity Award 2017, University of Idaho, USA.
- Best Poster Paper Award - EDAPS 2016 IEEE Conference
- DesignCon2016 Best Paper Award Finalist in Power Integriy in Power Distribution Networks track
- DesignCon2014 Best Paper Award Finalist in Interconnect Design track
- Tektronix President's Award Finalist in 2009 for developing the world's first 3D HDMI high speed serial signals.

IEEE ACTIVITIES

- Technical chair, IEEE Workshop on Microelectronics and Electron Devices, 2018
- IEEE member since 2015 and chair of IEEE EPS student chapter, Georgia Tech
- Represented LSI/Avago at IEEE Standards Association in projects- VNA S parameter and EM simulation.