Research Project

Interconnections and Assembly
Evaluate large glass BGA package-to-board reliability and investigate thermocompression bonding to ultra-thin substrates

Research Objectives
The objectives of this project are three fold

i. Second Level Interconnections (SLI) - Improve package-to-board pitch while compensating increased stress as the high-density interposers are developed with low-CTE substrates and as their size is increased from small to wafer-level packages to ultra-large interposers that are as big as 50mm in size.

ii. First Level Interconnections (FLI) - Demonstrate and characterize a high throughput thermocompression bonding process compatible for assembly on ultra-thin organic and glass substrates.

iii. SLI/FLI Integration - Perform reliability evaluation and study failure modes on comprehensive integration at first and second level interconnections.

In this project, my primary focus is on Board Level Interconnection and Assembly Reliability (BLIAR) investigating manganese (Mn) doped novel solder SACm0510 for balanced TCT and drop test performance, EPAG surface finish and IMC characterization at board level. Furthermore, for integration best known processes, materials and tools for SLI and FLI integration will be subsequently applied for technology transfer to mobile demonstrator.

Background
With the necessity to accommodate high I/O density, improve performance and implement miniaturization at low cost, a radical change in interposer design has been in focus. New interposers including low-CTE organics, silicon or glass along with low-CTE substrates and high dimensional stability are becoming critical for mobile and high-performance 2.5D packages. Such advanced packages are trending to low CTE and thus pose board-level interconnection reliability challenges due to the large CTE mismatch and smaller pitch. These problems are further aggravated with the trend to large (30-60 mm) packages. In addition, board-level interconnections should also be compatible with standard SMT processes. This trend is schematically shown in Fig. 1, from the traditional organic BGA package on board in Fig 1(a), to silicon interposer on organic BGA package on board 1(b), to the proposed R&D in direct-attach of low-CTE organics, silicon or glass to board in Fig 1(c).
Unique Approach
The strategy of the board-level I&A program is to explore, develop and demonstrate enhanced interconnection materials such as stress-relief interfaces, novel solders, new surface finish and underfills with considerations of overmolding.

1. Firstly, to meet the emerging needs along with innovative low-cost, SMT-compatible stress-management addresses to overcome the challenges associated with board-level interconnections. Such a strategy enables further system integration and miniaturization, by addressing challenges of large body size and enabling pitch reduction. Current R&D focus is on
   i. Innovative novel solder SACm0510 for balance thermomechanical and drop-test reliability in comparison to SAC 105 and SAC 305
   ii. EPAG evaluation and IMC characterization at board level

2. Secondly, redevelop stencil printing activity in PRC with optimized solder volume that is necessary to accommodate finer I/O pitches, requiring a finer control of IMC formation and growth during the assembly process to maintain the electrical and reliability performance

Interdisciplinary Research
For board level reliability – challenges and research addressing such challenges is listed in table 1

<table>
<thead>
<tr>
<th>Challenge</th>
<th>Research to Address Challenges</th>
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<tr>
<td>Assembly incorporating molding component</td>
<td>FEM Modeling to analyze warpage on SLI/FLI reliability and preliminary trials on glass</td>
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<tr>
<td>EPAG surface finish and IMC characterization at board level</td>
<td>New test vehicle with Si interposer with EPAG/Pallabond to enhance failure</td>
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### Results:

Using FEM simulations, warpage was modelled as a function of molding compound thickness and Si interposer thickness. Figure 3 (a) shows geometry of 700 um thick Si interposer with 300 um thick molding compound, 250 um diameter SAC 305 solder, 10 um thick Cu pad and 1mm PCB. Figure 3 (b) indicates at -40C the warpage is concave down primarily dominated by CTE of PWB, but at +125C, warpage response is nearly flat since CTE of mold compound negates CTE of PWB at higher temperatures. Additionally, thick overmold results in higher warpage at panel level before board level assembly with potential degradation of balling and assembly yield, and risks of panel cracking during overmold curing (shrinkage). Therefore, there is a necessity to find optimal interposer thickness that can be fabricated for a specified mold thickness. Figure 3(c) shows warpage with variation of interposer thickness: 100 um, 400 um and 700 um at two temperature extremes -40C and reflow 260C for 200 um and 300 um mold thicknesses.

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**Figure 3:**

(a) Geometry of overmolded Si-interposer with SAC 305 on PWB, (b) Warpage response at -40C and 125C, (c) Warpage as function of interposer thickness.