

# Majid Ahadi

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## Education:

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- **Georgia Institute of Technology**, Atlanta, GA, PhD Candidate, Electrical Engineering (minor in computer science), 2016 – 2020, GPA: 3.66, **Graduation: Sept. 2020**, Advisor: Professor Madhavan Swaminathan
- **Colorado State University**, Fort Collins, CO, Master's Degree, Electrical Engineering 2014 – 2016, GPA: 3.72
- **K.N.Toosi University of Technology**, Tehran, Iran, Bachelor's Degree, Electrical Engineering 2009- 2013, GPA: 3.6

## Skills:

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- **Hardware:** Signal and power integrity, Packaging, SerDes, Transmission lines, Digital and analog circuit design, PCB design, Signal processing, Electromagnetics, Microwave circuits, RF circuits, VLSI, Computer architecture.
- **Software:** C/ C++, Python, MATLAB, JavaScript, VHDL, Amazon Web Services, CUDA, OpenMP, Linux.
- **Machine Learning:** Supervised/ unsupervised learning, Reinforcement learning, Neural networks, Convolution neural networks, Recurrent neural networks, Deep learning, Online learning, Bayesian optimization.
- **Simulation:** High-speed Channels, Device and circuit modeling, Statistical analysis, ADS, Cadence, HSPICE, HFSS.
- **Other:** Visualization, Image processing, lab measurement (Oscilloscope, VNA, etc.).

## Work Experiences and Projects:

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- **Research Assistant** **Georgia Institute of Technology** 2017 – present
  - Inverse design of electronic systems with machine learning: Setting parameters in a complicated design using ML algorithms based on the desired output, to replace tedious tuning and sweeping strategies.
  - Quick analysis of SERDES channels using machine learning: Prediction of eye-diagram characteristics (Jitter, BER, etc.) for SERDES channels using polynomial chaos theory, Bayesian optimization and other ML methods (**In collaboration with IBM**)
  - **DARPA Common Heterogeneous Integration and IP Reuse Strategies (CHIPS):** As a member of this program, I developed interconnect and PDN models on Silicon and LCP interposers for 2.5 D packages, and performed signal and power integrity analysis.
  - Capacitor optimization for power delivery networks: Using the genetic algorithm to place decoupling capacitors in printed circuit boards.
  - Student member of the NSF Center for Advanced Electronics through Machine Learning (CAEML), 2016 - present
- **SIPI Intern** **Apple** Summer 2020
  - Developing numerical and machine learning algorithms for RF interference simulation in the signal and power integrity team.
- Opportunity Research Scholar's mentor **Georgia Institute of Technology** 2019 - 2020
  - Mentoring a group of undergraduate students on a research project.
- **Electrical Engineering Intern** **Cadence Design Systems** Summer 2018
  - Design space exploration: An efficient method was developed for design space exploration and sensitivity analysis of a DDR4 topology using Polynomial Chaos theory during **internship at Cadence**.
- Teacher Assistance **Georgia Institute of Technology** 2016
- **Research Assistant** **Colorado State University** 2014- 2016
  - Hyperbolic Polynomial Chaos (HPC) expansion for uncertainty quantification: A novel approach for alleviating curse of dimensionality in high dimensional stochastic problems based on HPC.
  - Uncertainty Quantification for High Speed Circuits: Developing numerical approaches to achieve speedup in stochastic analysis and simulation of high-speed circuits.
- **Electrical Engineering Intern** **Ansys, Inc.** Summer & Fall 2015
  - Quality Assurance of Nexxim: Writing MATLAB scripts for daily accuracy check of ANSYS circuit solver (Nexxim) by comparing daily results with a predetermined baseline during internship at ANSYS.
- Voluntary: Cultural mentor **Colorado State University** 2015
  - Holding social and cultural events and assistance to new international students.
- Electrical Engineer **Kianic Company** 2013



- M. Ahadi, A. K. Prasad, S. Roy “Hyperbolic Polynomial Chaos Expansion (HPCE) and its Application to Statistical Analysis of Nonlinear Circuits,” *IEEE International Conference on Signal and Power Integrity*, May 2016
- M. Ahadi, J. Hejase, W. Becker, M. Swaminathan “Development of Polynomial Chaos based Surrogate Models for Channel Simulation”, *IEEE Conference on Electromagnetic Compatibility, Signal & Power Integrity EMC+SIPI*, 2018
- M. Ahadi, H. Yu, J. Hejase, W. Becker, M. Swaminathan, “Polynomial Chaos modeling for jitter estimation in high-speed links”, *International Test Conference*, October 2018
- M. Ahadi, J. Hejase, W. Becker, M. Swaminathan “Jitter and Eye Estimation in SerDes Channels using Modified Polynomial Chaos Surrogate Models”, *IEEE EPEPS*, October 2018
- M. Ahadi, A. Varma, K. Keshavan, M. Swaminathan, “Design Space Exploration with Polynomial Chaos Surrogate Models for Analyzing Large System Designs”, *DesignCon 2019*, Jan. 2019
- M. Ahadi, J. Hejase, W. Becker, M. Swaminathan, “Eye Diagram and Jitter Estimation in SerDes Designs using Surrogate Models Generated with the Polynomial Chaos Theory”, *DesignCon 2019*, Jan. 2019
- M. Ahadi, A. Varma, K. Keshavan, M. Swaminathan, “A Modified Polynomial Chaos Modeling Approach for Uncertainty Quantification”, *International Applied Computational Electromagnetics Society (ACES) Symposium*, April 2019 (Invited paper to special session)
- K. Roy, M. Ahadi, H. Torun, R. Trincherro, M. Swaminathan, “Inverse Design of Transmission Lines with Deep Learning”, *IEEE Conference on Electrical Performance of Electronic Packaging and Systems*, October 2019
- R. Trincherro, M. Ahadi, K. Roy, M. Swaminathan, F. G. Canavero, “Design of High-Speed Links via a Machine Learning Surrogate Model for the Inverse Problem”, *IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)*, Kaohsiung, Taiwan, 2019
- M. Ahadi, M. Swaminathan, “Determining worst-case eye height in low BER channels using Bayesian optimization.”, *LASCAS 2020 - 11th IEEE Latin American Symposium on Circuits and Systems*, San José, Costa Rica, 2020.