

**Topic: System Level Packaging:** Interconnections Reliability and Failure Modes

**Overview:** System-level packaging includes chip- and board-level assembly. Chip-level assembly focuses on connecting a silicon chip to a substrate and board-level assembly focuses on assembling this chip-level package to a printed circuit board for end use application. While designing a system-level package, it is critical to understand the thermomechanical failure mechanisms and reliability of both chip- and board-level interconnections, along with their interdependencies. This short course will discuss the importance of reliability for a system-level package, introduce the different failure modes commonly observed in chip- and board-level interconnections and finally, explore recent developments made to address these challenges.

**Instructor Bio:** Vidya Jayaram received her M.S. in Materials Science and Engineering at the 3D Systems Packaging Research Center at Georgia Institute of Technology, USA under the guidance of Prof. Rao Tummala and Prof. Vanessa Smet. and B. Tech degree in Polymer Engineering and Technology from the Institute of Chemical Technology, Mumbai, India in 2015. Vidya is currently working at Intel Corporation in Chandler, Arizona as a Materials Technology Development Engineer. Her work at Intel has been focused on process and material development of capillary underfills, wafer-level fan-out packaging and thermal solutions for advanced packaging. Vidya is an active member of the ECTC Materials and Processing Committee and the Chair for Automotive, 5G & Next Gen Applications Session at IMAPS Device Packaging Conference.