Enabling chip-to-substrate all-Cu interconnections: design of engineered bonding interfaces for improved manufacturability and low-temperature bonding

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***Abstract* – This paper presents the design and implementation of engineered nanoscale bonding interfaces as an effective strategy to improve manufacturability of Cu-Cu bonding to the level where it can, for the first time, be applied to chip-to-substrate (C2S) assembly. All-Cu interconnections are highly sought after to meet the escalating electrical, thermal, and reliability requirements of a wide range of emerging digital and analog systems. Such applications require low-cost processes with bonding temperatures and pressures ideally below 200°C and 20MPa, respectively, far from existing solutions established in wafer-level packaging. GT-PRC and its industry partners address this technology gap through innovative designs of bonding interfaces, introducing: 1) novel ultra-thin surface finish metallurgies applied on Cu bumps and pads to prevent oxidation and achieve low-temperature assembly; 2) low-cost fly-cut planarization technique to lower bonding pressures; and 3) low-modulus nanocopper foam caps to provide tolerance to non-coplanarities, and further reduce bonding temperatures and pressures.**

Keywords – Cu interconnections, flipchip bonding, fine pitch, thermocompression, surface finish, planarization, nanocopper, nanoporous Cu, sintering, coarsening etc.

I. INTRODUCTION

THE ever-increasing requirements for higher I/O density, performance, and miniaturization at low cost in emerging high-performance computing systems, with benefits of low power consumption, is projected to drive the off-chip interconnection pitch to 20µm and below in the next 5 years. This pitch-scaling trend has been reinforced through adoption of advanced packaging solutions such as 2.5D interposer packages and 3D IC integration in computing applications. This is, in turn, being driven by a mutual convergence of semiconductor design limitations coupled with assembly and interconnection advances. This aggressive pitch scaling to below 20µm has pushed solder-based interconnections, including the current Cu pillar technology [1], to their limits, in terms of electrical, thermal and reliability performances. Pitch scaling is accompanied by a reduction in solder volume and bump diameter to prevent bridging, bringing unprecedented stress management challenges. Moreover, by 2020, ITRS has predicted that high bandwidth computing in high-end processors will invoke complementary trends such as current densities exceeding 10^5A/cm^2 with shrinking interconnection diameters, and thermal stability requirements at temperatures over 150^{o}C, beyond the capability of standard solder alloys. With the explosive growth in automotive electronics, similar trends towards high-current densities and operating temperatures have also been observed in analog applications. This has cast further doubt on whether solder-based interconnection technologies can meet the performance and reliability requirements of next-generation high-performance systems.

Intensive research has been carried out to extend applicability of solders to finer pitches on account of their ease of processability and low cost. Alternative technologies like transient liquid phase bonding [2] and solid-liquid interdiffusion (SLID) bonding [3] have been proposed, which essentially bring about full conversion of solder to an intermetallic phase with higher power handling capability and thermal stability. Although implemented in limited volume manufacturing [4], SLID bonding in the Cu-Sn system faces challenges of high assembly cycle times, and reliability issues on account of Kirkendall voiding and intermetallic brittleness [5]. As a result, solid-state interconnection technologies without solders are gaining momentum to achieve targeted pitch and performance goals.

Solid-state bonding, however, inherently possesses high stiffness and low interdiffusion rates, thus necessitating high pressures or ultrasonic energy, and high temperatures to initiate contact, break surface oxides and form a metallurgical bond at the interface. These processes generally carry a high

thermal and force budget thus severely limiting the throughput of solid-state interconnections and hindering wide adoptability. Gold is a serious candidate to develop soft deformable interfaces and as a result Au-stud bumps and Au-Au interconnections (GGI) have been demonstrated using ultrasonic and thermocompression bonding at bump pitches as low as 20µm [6-8]. However, despite their outstanding electrical, thermal, and reliability performance, GGIs are not used extensively in high-volume manufacturing (HVM) due to the prohibitive cost of Au.

Accordingly, all-Cu interconnections without solders have been highly sought after by the microelectronics industry as the ultimate interconnection node for its low cost yet superior thermal and electrical performance. Copper provides excellent power-handling capability, high-speed signal transmission and is compatible with standard back-end-of-line (BEOL) infrastructures [9, 10]. However direct Cu-Cu bonding suffers from 3 major material challenges: 1) room-temperature oxidation; 2) low-diffusivity of Cu at low temperatures required in assembly; and 3) relatively high Young's modulus, giving low tolerance to non-coplanarities, non-uniform stress distribution across the low-k dielectric stack and warpage concerns. On account of these processability concerns, these technologies are currently limited to low-volume wafer-scale packaging including chip-on-chip (CoC), wafer-on-wafer (WoW) and chip-on-wafer (CoW) assembly across 3D-ICs and memory applications [10]. This paper first reviews current state-of-the-art of wafer-level Cu-Cu bonding and introduces the manufacturability gap for applicability at package level. Requirements for chip-to-substrate (C2S) all-Cu interconnections are then extracted and addressed with two innovative technologies relying on design of bonding interfaces at nanoscale.

II. Direct Cu-Cu Bonding Technology Review And Strategy for Manufacturability

Current direct Cu-Cu bonding technologies rely heavily on selective activation of the bonding surface to improve quality of the metallurgical bonding, as well as involve expensive planarization steps to improve planarity of the interface and provide tolerance to non-coplanarities. There have been many reports on surface-activated bonding (SAB), involving a pre-bonding Ar^+ ion sputtering step in ultra-high vacuum (>10^{-8} Torr) environments to chemically activate the Cu surface and bonding under vacuum at ambient temperature to form a metallurgical bond [11]. Other surface activation practices involve forming an organic self-assembled monolayer (SAM) [12] that protects the Cu surface from oxidation and later volatizes under high bonding pressures and temperatures to form an oxide-free bonding interface. Chemical-mechanical-polishing (CMP) is also utilized in direct Cu-Cu bonding in order to improve the surface roughness and hence contact area of the interface [13-17]. Under high-temperatures (>350ºC) and pressures, surface oxides break up and bonding interfaces mate perfectly after a post-anneal step. Essentially, current state of the art technologies in direct Cu-Cu bonding require high bonding forces, assembly in vacuum or inert environments with temperatures far greater than that used for solder-based reflow, long annealing times with an expensive CMP step, thus limiting their adoption to wafer-level packaging (WLP) only. Furthermore, these bonding approaches have very low tolerance to substrate warpage and bump non-coplanarities, that are invariably present during IC assembly onto interposer and package substrates. Besides, the bonding pressures need to be limited to <20MPa and <250ºC respectively for C2S assembly to prevent failures in low-k layers on the die and comply with current substrate material limitations. Assembly of stiff all-Cu interconnections onto brittle ultra-thin glass substrates present yet another challenge [18]. As a result, from the point of view of C2S, there exists an I/O pitch and performance gap, with low-performance solder-based interconnections at one end of the spectrum, and high-performance, high-cost, low throughput solid-state interconnections at the other as illustrated in Figure 1.

Fundamentally, highly-reliable C2S interconnections, should possess the high electrical and thermal performance of copper along with the wettability and compliance of solder to enhance bonding manufacturability and improve tolerance to non-coplanarities and warpage. Recently, novel interconnections based on capillary bridging of nano-Cu ink under evaporation to form interconnected necks were demonstrated by IBM Zurich [19]. Development of nanoparticle-based interconnects have also gained momentum in the past few years [20], thus casting nanomaterials as key enablers to achieve strong joints, high electrical and thermal performance, low-temperature bondability and tolerance to non-coplanarities and warpage. However, the technology readiness of nano-pastes and inks is questioned [21], on account of: 1) limited pitch-scalability; 2) retained porosity post-sintering; 3) stress management; 4) expensive surface treatments of nanoparticles to prevent their oxidation. As a result, a new class of Cu interconnections with optimized bonding nanoscale interfaces is required to bridge the pitch scaling gap with improved performance and reliability.

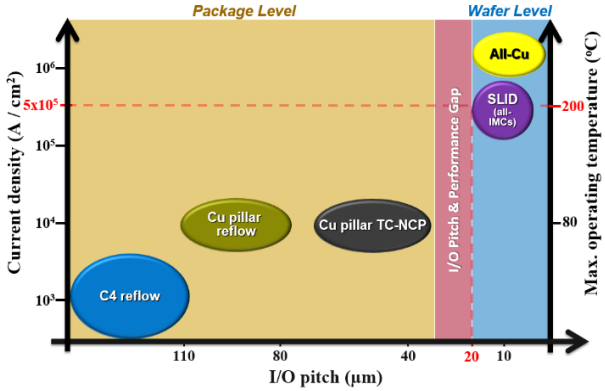

Figure 1. Metrics for off-chip interconnection pitch and performance scaling in advanced packaging

GT-PRC has recently pioneered two novel assembly technologies (as shown in Figure 2) as a part of its roadmap to address the aforementioned challenges through design and nano-engineering of the bonding interfaces [22, 23]. The primary objective towards GT – PRC's novel approach is to demonstrate all-Cu interconnections without solders at low bonding temperatures (<250ºC) and low pressures (<20MPa) with improved assembly manufacturability. In the first approach, the bonding interfaces consist of thin-film electroless Pd – autocatalytic Au (EPAG) surface finish, ~300nm in thickness, applied on Cu bumps and pads. Cu-EPAG interconnections, therefore, benefit from the oxidation prevention and enhanced processability of Au in bonding, while retaining most of the properties of Cu. In order to improve interconnection compliance, a low-cost planarization technique by fly-cut bit grinding technique is also introduced to control bumps non-coplanarities to within 1µm over a 300mm wafer. While these improvements enable scaling of all-Cu interconnections to bonding pressures of about 75 MPa, further innovations from material design standpoint are required to further reduce the bonding pressures and bonding temperatures for applicability to large die sizes with increasing I/O densities. To overcome this, GT – PRC has proposed a second approach, in which the bonding interfaces consist of low-modulus nanocopper foam caps to form strong all-Cu interconnections by low-temperature and low pressure bonding with the following attributes: 1) sub-20GPa Young's modulus as synthesized to provide high tolerance to surface roughness, non-coplanarities, and warpage; 2) low-cost fabrication processes compatible with standard lithography processes; 3) pitch scalability given by solid-state bonding; 4) highly-reactive nano-surfaces enabling low-temperature densification to bulk copper. This paper reviews the current progress in both approaches and positions them fundamentally in contrast to the state of the art in Cu bonding technologies.

III. Cu Interconnections with Thin Surface Finish and Low-Cost Planarization

The first approach features the following key innovations in bonding interfaces to form Cu interconnections without solders at T < 250ºC, in air, without complex surface preparation [24]: 1) preventing copper oxidation by metallic surface finish on Cu pillars and pads; 2) accommodation of bump and pad non-coplanarities by controlled collapse under pressure during thermocompression bonding; 3) superior thermomechanical reliability on low-CTE organic and glass packages and electromigration resistance at 10^6 A/cm^2 with stable metallurgical interfaces; and 4) high-throughput assembly with cycle times <5sec using pre-applied underfill. In previous results, a 3X reduction in bonding pressures to 120MPa has been established by changing the surface finish from the stiff 3µm electroless Ni – 250nm immersion Au (ENIG) to the thin and deformable 100nm electroless Pd – 250nm autocatalytic Au (EPAG) [22]. This novel Ni-free surface finish, developed by Atotech GmbH, is suitable for high-performance applications with improved high-frequency performance and high-density routing at sub-10µm interconnect pitches, thus meeting the needs of ultra-fine pitch architectures [25].

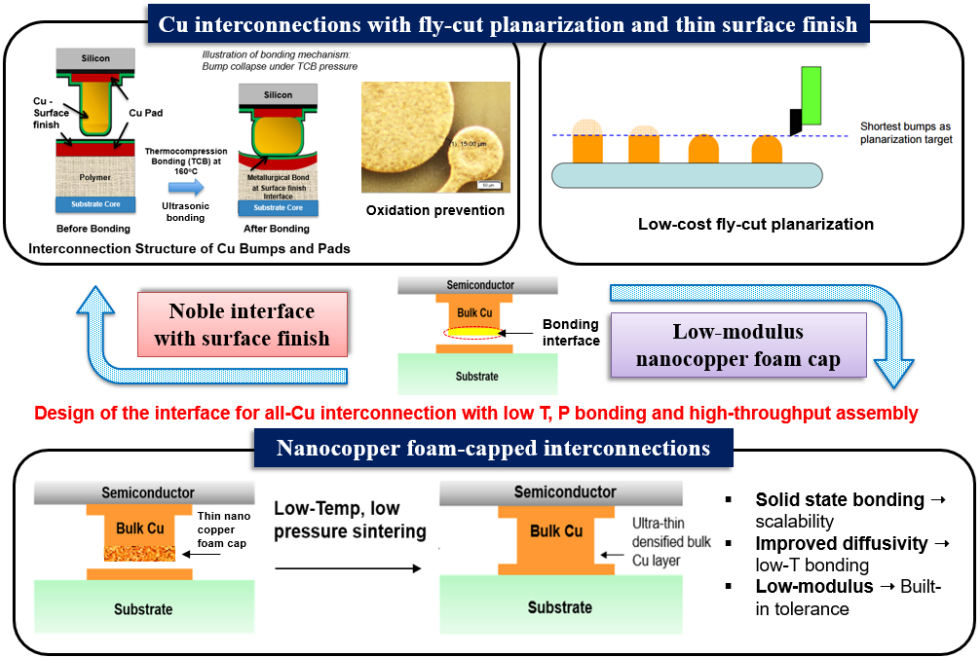

Figure 2. Unique GT – PRC approaches towards all-Cu interconnections without solders

Although the performance and reliability benefits have been adequately represented in our previous work [26-28], this work succinctly focuses on the nature of the bonding interface using thin EPAG surface finish.

A. Interdiffusion in the Cu-Pd-Au System

While it is well-known that the self-diffusivity of Cu is quite low [29] at <200ºC, thus leading to processability challenges in direct Cu-Cu bonding, Cu atoms have a relatively high diffusivity into an Au matrix [30]. This is generally mediated through defect paths via grain boundaries in nanoscale grains, surface paths on account of curvature of the asperities and through the lattice thus giving grain boundary, surface and bulk diffusion paths respectively. Thus, there is a need for an adequate barrier layer to prevent Cu atoms of the Cu bumps from diffusing through the thin Au layers to form intermetallics and CuO in the bulk and on the surface of Au respectively. Using a simple analytical diffusion model between a binary Cu-Pd [31, 32] and Cu-Au couple, it is observed that 100nm Pd allows Cu to diffuse through defect paths to the Pd surface within 4 minutes above 200ºC while Cu diffuses through 250nm of Au within 22 hours to from CuO at its surface. Formation of a surface oxide of Cu can seriously degrade the bonding interface as well as interconnect reliability under operating conditions, thus stressing the need for high contact area and lower surface roughness at the bonding interface to prevent formation of Cu oxide in the voids. On the other hand, having perfect contact can initiate formation of Cu-Au intermetallic compounds at the interface under prolonged ageing conditions [30, 33-36], which can also degrade the reliability of the interface. It has been shown that under prolonged ageing conditions, a stable intermetallic AuCu (50-50 at%) is formed [36]. Other studies have reported that AuCu is ductile in nature on account of its lattice structure ($L1_o$) [37] in contrast to brittle solder-based intermetallics (Cu_3Sn and Cu_6Sn_5) and can thus stabilize the microstructure at the bonding interface and provide adequate reliability.

B. Assembly and bonding chracterization

In order to test our initial assessment, a 40µm-pitch test vehicle (TV) consisting of a Si die with electroplated Cu pillars 13µm in height and 20µm in diameter was assembled on non-patterned Si substrates with blanket Cu by flip-chip thermocompression bonding. EPAG surface finish was applied on Cu bumps and substrate metallization. To ensure adequate metallurgical bonding between the Au-Au interfaces, assembly was carried out at 250ºC for 5min with the bonding pressure varied from 100-300MPa. A total of 15 assemblies were built for this study. A maximum bonding strength of 118 ± 53MPa was observed at a bonding pressure of 300MPa for the as-plated assemblies. The high deviation in shear strength was attributed to non-uniform contact area during bonding causing voids. The cross-sectional SEM image of an as-bonded assembly of Cu bumps on pad with pre-applied underfill in Figure 3 illustrates this. Results of thermal ageing studies on 26 TVs assembled at 300MPa, carried out at 200ºC for 1000 hours are as shown in Figure 4. A continuous drop in shear strengths to 26 ± 6.2MPa at 1000 hours was observed for the as-plated assemblies. A further SEM-EDS analysis of the sheared substrate interface shown in Figure 5 indicated the presence of CuO formed under thermal oxidation of the non-contacted areas as well as AuCu intermetallic at the contacted surfaces, thus validating the predictions of the diffusion model. Insufficient contact caused Cu to diffuse through defect paths and form brittle CuO which further degrades the strength of the interface, ultimately causing failure at the Au – CuO interface. Although the presence of a highly deformable Au surface finish improves diffusivity and ambient bond strength of the proposed technology, there is an acute need to improve the contact area under bonding to decrease the surface asperities and prevent diffusion of Cu to the Au surface and its subsequent oxidation.

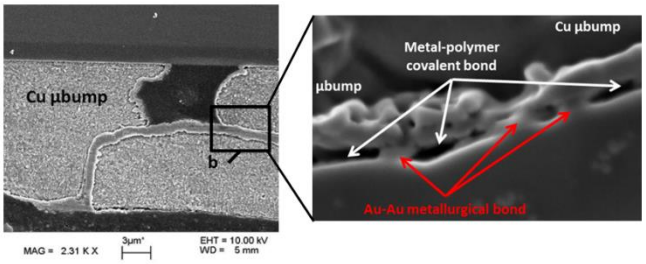

Figure 3. SEM cross-section of as-plated Cu bump-on-pad asseembly with pre-applied underfill trapped in interfacial voids

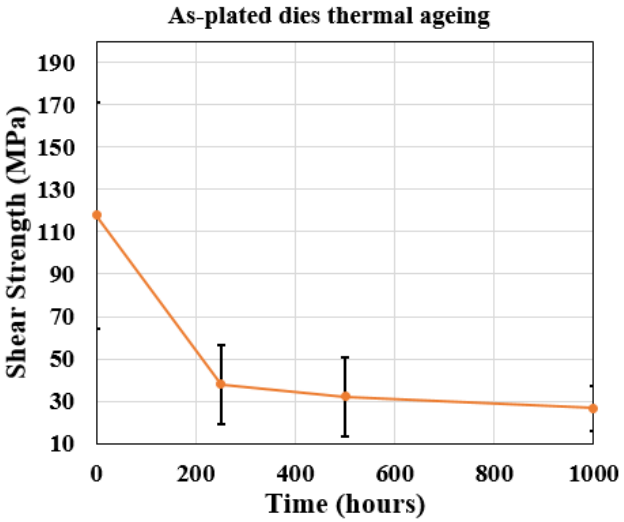

Figure 4. Shear strengths of assemblies with as-plated Cu bumps over isothermal ageing at 200ºC – 1000hours

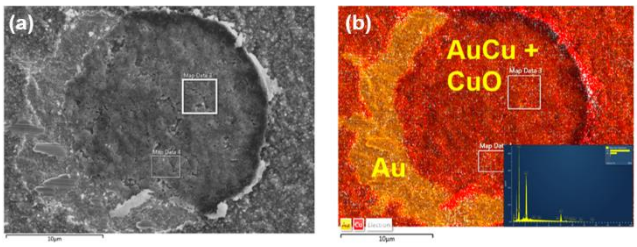

Figure 5. SEM-EDS of the sheared substrate interface aged isothermally at 200ºC for 1000 hours

Further, as pitch scaling continues to 20µm and below, the die-attach photoresist pattern becomes increasingly complex, and controlling the fine feature heights of the plated Cu bumps becomes difficult. This variation in bump height can cause non-uniform distribution of applied pressure across the Cu traces on the substrate. This causes a rippling effect during Cu-Cu bonding as demonstrated in [38]. In the next section, we consider a unique low-cost planarization process to improve the tolerance to non-coplanarities and enhance the contact area during bonding.

C. Low-cost planarization

Si dies with planarized Cu bumps were fabricated using Disco's low-cost fly-cut planarization tool. This surface planer removed all within-feature non-uniformities and asperities including the rough surface to provide a through-thickness variation of <1µm on a 300mm wafer. On assembly, the test vehicles with planarized Cu bumps showed a maximum shear strength of 196 ± 2.6MPa. This shear strength is similar to the cohesive shear strength of copper itself (190MPa), thus providing an established benchmark for bond strengths. On this account, 26 more test vehicles with planarized Cu bumps were assembled at bonding pressure of 300MPa for thermal ageing studies at 200ºC – 1000 hours to compare with the previous results using as-plated Cu bumps. A sudden drop in shear strength to 62MPa was observed at 250 hours after which the shear strength stabilized to 40MPa (comparable to Sn-Ag solders) at 1000 hours. This comparison between the thermal ageing performance of the assemblies with as-plated and planarized Cu bumps has been shown in Figure 6. SEM imaging of the sheared substrate interface confirmed a ductile failure at the bonding interface evident from the dimpled morphology while SEM-EDS established the presence of only Au and AuCu intermetallic at the bonding interface as shown in Figure 7. Thus, formation of a stable ductile AuCu phase through Cu-Au interdiffusion caused degradation of the shear strengths and failure at the Au-AuCu interface at 250 hours. However, the presence of a stable AuCu phase and the absence of the brittle CuO phase due to better contact area caused stabilization of the microstructure and improved reliability of the bonding interface under thermal ageing over 1000 hours. Through Finite Element Modeling (FEM) studies, it was also observed that using flat planarized bumps in contrast to rounded as-plated bumps redistributes the applied pressure at the interface thus preventing stress concentrations at the Cu pad – substrate interface and improving package reliability.

While we can see that this surface finish technology in conjunction with low-cost planarization enables significant scaling of the bonding pressure down to 75MPa [22] and improved thermal reliability, a complete redesign of the material system is required to scale the bonding pressure below 20MPa to enable the targeted near pressure-less process along with adequate tolerance to non-coplanarities and warpage.

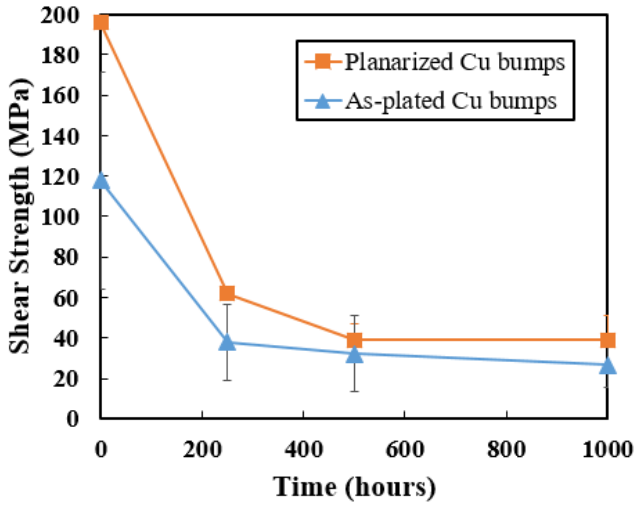

Figure 6. Comparative shear strengths of assemblies with as-plated and planarized Cu bumps over isothermal ageing at 200ºC – 1000hours

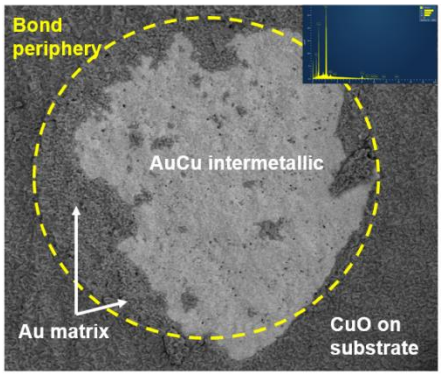

Figure 7. BSE-SEM of sheared substrate interface with planarized die aged isothermally at 200ºC – 1000hours with SEM-EDX elemental chart as inset

IV. NANOCOPPER FOAM INTERCONNECTIONS

There is a need to develop a low-modulus solid-state interconnection that will possess the performance of copper and the processability of solder to meet the target bonding parameters and warpage compliance. To tackle these challenges, GT-PRC proposes nanocopper foams as the second approach towards modification of the bonding interfaces. These nanocopper foams can replace traditional solder caps to form nano-Cu foam-capped interconnections through solid-state sintering at bonding pressures <20MPa and T < 250ºC. In this technology, the traditional solder caps are replaced by nanocopper foams with the following attributes: 1) tailorable sub-20GPa elastic modulus as-synthesized; 2) fabrication by plating and dealloying compatible with standard lithography processes; 3) pitch scalability on account of solid-state bonding; and 4) highly-reactive nano surfaces enabling sintering and low-temperature densification to bulk Cu. We have previously demonstrated an initial proof-of-concept of nanocopper foam interconnections [23] and will be reviewing further progress towards manufacturability of these novel systems in the next sections

A. *Synthesis and fabrication*

The primary and most common method to synthesize nanocopper foams is through dealloying or selective etching of an alloy in a corrosive environment. Under favorable conditions, electrochemically nobler elements are etched away and the remnant solid fraction of the alloy self-assembles into a three-dimensional interconnected network of ligaments and junctions at nanoscale [39, 40]. In this work, nanocopper foams were synthesized via two methods: 1) co-sputtering and dealloying; and 2) stack-plating, annealing and dealloying. Diced sections of a Si substrate co-sputtered with 2µm of amorphous $Cu_{25}Si_{75}$ thin film (Figure 8(a)) were electrochemically dealloyed in 3% hydrofluoric acid (HF) under an external potential of -0.3V (with respect to a saturate calomel electrode as reference) to form a 3D nanoporous structure of Cu. SEM imaging of the foams presented a 3D bi-continuous morphology with interconnected junctions and ligaments as shown in Figure 8(b). The as-fabricated foams exhibited an average ligament size of 35nm with a through-thickness shrinkage of about 22.5% from an initial thickness of 2µm for the Cu-Si films. Using java-based ImageJ [41], image processing on the thresholded SEM images gave a relative density of 60% ± 2% of the nano-Cu foam.

While co-sputtering and dealloying provides uniform nano-Cu foams, we have also looked at electrodeposition of Cu-based alloys to develop more manufacturable routes towards fabricating and patterning nano-Cu foams that are compatible with standard lithography processes. The Cu-Zn binary alloy system was identified as the best compromise between electrochemical potential difference and ease of processability, to form nano-Cu foams. Accordingly, a $Cu_{30}Zn_{70}$ alloy composition was selected based on previous literature [42-45] to give a uniform isotropic nano-Cu foams. Currently a stack-plating approach towards alloy formation is followed. Zn was electrodeposited onto 18um thin pure Cu sheets (5.5x1.5 cm^2) using a 3-electrode setup with two pure-Zn sheets acting as the front and rear anodes and the Cu sheet acting as the cathode in a buffered $ZnSO_4$ electrolyte. The current densities were appropriately adjusted to uniformly deposit equal layers of Zn on both sides of the Cu sheet so as to make up the required weight for a $Cu_{30}Zn_{70}$ composition. Further, annealing was carried out at 250°C for 8 hours to homogenize the alloy. Free dealloying was carried out in 5% HCl solution for 12.5 hours to form a bi-continuous network of fine-nanocopper foam (25-30nm feature size) and coarse-nanocopper foam (300-500nm feature size) as can be seen in Figure 8(c)-(d). This process is currently undergoing additional optimization to improve uniformity of the nanocopper foams. While stack-plating is the most convenient way towards electroplated nano-Cu foams, we are also working on co-deposition of Cu-Zn simultaneously to improve the homogeneity of the deposited alloy as well as enable standard patterning processes and further improve manufacturability.

B. *Free-sintering and assembly*

Free-sintering trials of the as-fabricated foams were carried out under N_2 and forming gas (N_2 – 5%H_2) environments to observe coarsening and densification behavior. Sintering in

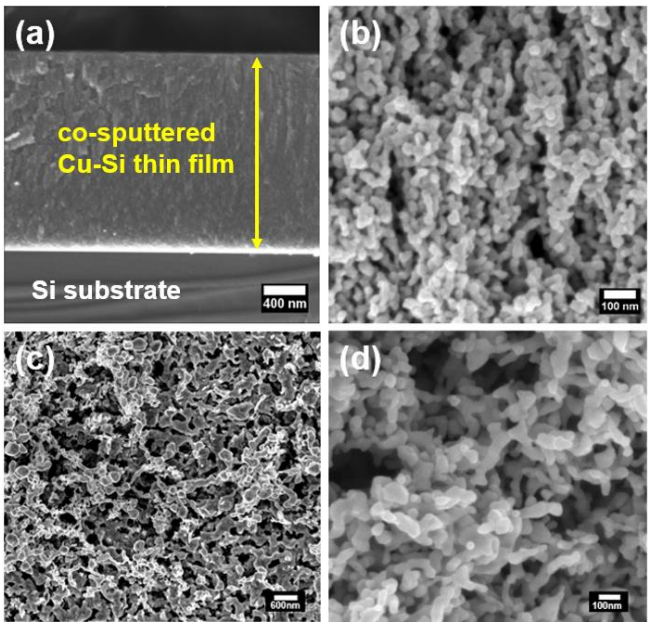

Figure 8. Cross-sectional SEM images of (a)-(b) co-sputtered Cu-Si thin film and dealloyed nano-Cu foam; plan-view SEM images of (c) macro-Cu foam and (d) nano-Cu foam from dealloyed Cu-Zn

N_2 environment at 300°C-60min resulted in an average increase in junction size from 30nm to 55nm with no significant change in the height of the foam. However, sintering under forming gas for 300°C – 60min increased these dimensions to about 150nm with a significant reduction in foam height to about 1.3µm. The relative density of the foam was estimated to be around 90% due to the large amounts of densification and coarsening observed in the foam. This wide disparity in feature sizes during sintering under N_2 and forming gas environments suggested formation of hard Cu oxides under N_2 environment that prevented further coarsening and densification processes. While under forming gas, a standard reducing atmosphere used in the industry, surface oxides were instantaneously reduced, thus promoting diffusivity and densification of the foams.

In order to assess the bonding characteristics of the nano-Cu foams to Cu traces under assembly conditions, thermocompression bonding assembly was carried out using a 6mm^2 blanket film of nano-Cu foam on Si substrate that acted as the die onto a cleaned 10x10 mm^2 Si substrate with blanket bare-Cu metallization. The foams were cleaned with acetic acid prior to the bonding to clean the ambient oxidation of the nano-surfaces [23]. The bonding was carried out in a chamber flooded with forming gas at 200 and 250°C for 15minutes at a bonding pressure of 9MPa. From the images in Figure 9, it can be seen that adequate bonding was achieved, for the first time, between the nano-Cu foam and the rough bare-Cu metallization with 85% and 90% in-plane density achieved for the parts bonded at 200°C and 250°C respectively. A preliminary shear strength of 4.2kgf was observed for the sample bonded under 9MPa – 250°C – 15min, thus passing industry standard specifications (MIL-STD-883G).

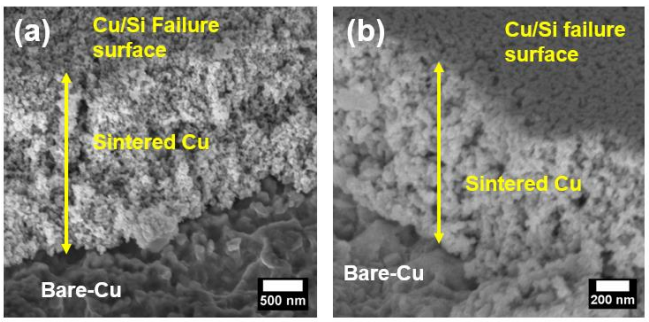

Figure 9. SEM cross-sectional view of fractured sintered nano-Cu joint on bare-Cu assembly at (a) 200ºC and (b) 250ºC

On failure analysis of the sheared joint at 200ºC, failure was mainly observed through the thickness of the sintered foam resulting in a shear through the foam thickness, while for the assembly bonded at 250ºC, failure was more prominent at the Cu/Si interface thus exhibiting improved densification of the foam. Further optimization of the trials is being carried out on planarized low roughness bare-Cu metallization to improve the densification behavior and associated bondability of the nano-Cu foams, to a level, where it can be applicable to C2S assembly.

V. Summary and Conclusions

This paper presented a brief overview of the need for novel solid-state bonding technologies as advances in computing applications push the off-chip interconnection pitch to 20µm and below. A case for Cu-Cu interconnections as the ultimate interconnection node was presented and the current state-of-the-art in direct Cu-Cu bonding technologies was reviewed. The high processability costs of solid-state interconnections used in WLP combined with inability of solders to cope with pitch scaling has led to an I/O pitch and performance gap. In view of this, GT – PRC's novel approaches to all-Cu interconnections without solders through design of nanoscale bonding interfaces towards enabling C2S applications were detailed. Using a unique thin EPAG surface finish, coupled with a low-cost fly-cut planarization technique, the bonding pressures and temperatures have been reduced to 75MPa and 250ºC respectively. Furthermore, improved reliability of assemblies with planarized Cu bumps has been demonstrated with the formation of a stable Au – AuCu intermetallic interface under 1000 hours of thermal ageing. In order to further enhance manufacturability and improve tolerance to non-coplanarities and warpage, low-modulus nanocopper foam-capped interconnections are introduced with the advantages of design flexibility, pitch scalability and reactive bonding interfaces. The fabrication, patternability and bonding readiness of the nanocopper foams are explored with the first successful assembly demonstration at 9MPa – 200ºC – 15min. Further research is being carried out to understand the fundamental sintering kinetics and densification mechanisms to design improved fabrication, patternability and assembly processes.

In conclusion, this paper presents novel, manufacturable, and low-cost Cu interconnection technologies with nano-engineered bonding interfaces to enable a first demonstration of Cu-Cu bonding in C2S applications and its positioning as a manufacturable and reliable technology towards high-performance applications.

Acknowledgments

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References

[1] M. Gerber, C. Beddingfield, S. O. Connor, M. Yoo, M. Lee, D. Kang, *et al.*, "Next generation fine pitch Cu Pillar technology — Enabling next generation silicon nodes," in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, 2011, pp. 612-618.

[2] H. A. Mustain, W. D. Brown, and S. S. Ang, "Transient Liquid Phase Die Attach for High-Temperature Silicon Carbide Power Devices," *Components and Packaging Technologies, IEEE Transactions on*, vol. 33, pp. 563-570, 2010.

[3] Z. X. Zhu, C. C. Li, L. L. Liao, C. K. Liu, and C. R. Kao, "Au–Sn bonding material for the assembly of power integrated circuit module," *Journal of Alloys and Compounds*, vol. 671, pp. 340-345, 6/25/ 2016.

[4] R. Agarwal, W. Zhang, P. Limaye, R. Labie, B. Dimcic, A. Phommahaxay, *et al.*, "Cu/Sn microbumps interconnect for 3D TSV chip stacking," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 858-863.

[5] K. Zeng, R. Stierman, T.-C. Chiu, D. Edwards, K. Ano, and K. N. Tu, "Kirkendall void formation in eutectic SnPb solder joints on bare Cu and its effect on joint reliability," *Journal of Applied Physics*, vol. 97, p. 024508, 2005.

[6] X. F. Ang, G. G. Zhang, J. Wei, Z. Chen, and C. C. Wong, "Temperature and pressure dependence in thermocompression gold stud bonding," *Thin Solid Films*, vol. 504, pp. 379-383, 5/10/ 2006.

[7] C. F. Luk, Y. C. Chan, and K. C. Hung, "Development of gold to gold interconnection flip chip bonding for chip on suspension assemblies," *Microelectronics Reliability*, vol. 42, pp. 381-389, 3// 2002.

[8] G. G. Zhang, X. F. Ang, Z. Chen, C. C. Wong, and J. Wei, "Critical temperatures in thermocompression gold stud bonding," *Journal of Applied Physics*, vol. 102, p. 063519, 2007.

[9] Y. H. Hu, C. S. Liu, M. J. Lii, K. J. Rebibis, A. Jourdain, A. L. Manna, *et al.*, "3D stacking using Cu-Cu direct bonding," in *3D Systems Integration Conference (3DIC), 2011 IEEE International*, 2012, pp. 1-4.

[10] Y.-S. Tang, Y.-J. Chang, and K.-N. Chen, "Wafer-level Cu–Cu bonding technology," *Microelectronics Reliability*, vol. 52, pp. 312-320, 2// 2012.

[11] T. H. Kim, M. M. R. Howlader, T. Itoh, and T. Suga, "Room temperature Cu–Cu direct bonding using surface activated bonding method," *Journal of Vacuum Science & Technology A*, vol. 21, pp. 449-453, 2003.

[12] C. S. Tan, D. F. Lim, X. F. Ang, J. Wei, and K. C. Leong, "Low temperature CuCu thermo-compression bonding with temporary passivation of self-assembled monolayer and its bond strength enhancement," *Microelectronics Reliability*, vol. 52, pp. 321-324, 2// 2012.

[13] X. F. Ang, A. T. Lin, J. Wei, Z. Chen, and C. C. Wong, "Low Temperature Copper-Copper Thermocompression Bonding," in *2008 10th Electronics Packaging Technology Conference*, 2008, pp. 399-404.

[14] E.-J. Jang, J.-W. Kim, B. Kim, T. Matthias, and Y.-B. Park, "Annealing temperature effect on the Cu-Cu bonding energy for 3D-IC integration," *Metals and Materials International*, vol. 17, pp. 105-109, 2011.

[15] J. Lannon, C. Gregory, M. Lueck, A. Huffman, and D. Temple, "High density Cu-Cu interconnect bonding for 3-D integration," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 355-359.

[16] B. Rebhan, G. Hesser, J. Duchoslav, V. Dragoi, M. Wimplinger, and K. Hingerl, "Low-Temperature Cu-Cu Wafer Bonding," *ECS Transactions*, vol. 50, pp. 139-149, March 15, 2013 2013.

[17] W. Ruythooren, A. Beltran, and R. Labie, "Cu-Cu Bonding Alternative to Solder based Micro-Bumping," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 315-318.

[18] V. Sukumaran, T. Bandyopadhyay, V. Sundaram, and R. Tummala, "Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, pp. 1426-1433, 2012.

[19] J. Zurcher, K. Yu, G. Schlottig, M. Baum, M. M. Visser Taklo, B. Wunderle, *et al.*, "Nanoparticle assembly and sintering towards all-copper flip chip interconnects," in *Electronic Components and Technology Conference (ECTC) , 2015 IEEE 65th*, 2015, pp. 1115-1121.

[20] K. Schnabl, L. Wentlent, K. Mootoo, S. Khasawneh, A. A. Zinn, J. Beddow, *et al.*, "Nanocopper Based Solder-Free Electronic Assembly," *Journal of Electronic Materials*, vol. 43, pp. 4515-4521, 2014/12/01 2014.

[21] K. S. Siow, "Are Sintered Silver Joints Ready for Use as Interconnect Material in Microelectronic Packaging?," *Journal of Electronic Materials*, vol. 43, pp. 947-961, 2014.

[22] N. Shahane, S. McCann, G. Ramos, A. Killian, R. Taylor, V. Sundaram, *et al.*, "Modeling, design and demonstration of low-temperature, low-pressure and high-throughput thermocompression bonding of copper interconnections without solders," in *Electronic Components and Technology Conference (ECTC) , 2015 IEEE 65th*, 2015, pp. 1859-1865.

[23] N. Shahane, K. Mohan, and A. A. Rakesh Behera, PM Raj, Vanessa Smet, Rao Tummala, "Novel high-temperature, high-power handling all-Cu interconnections through low-temperature sintering of nanocopper foams," in *IEEE Electronic Components and Technology Conference (ECTC) 2016*, 2016, p. Submitted.

[24] N. Kumbhat, A. Choudhury, V. Sundaraman, and R. R. Tummala, "Interconnect assemblies and methods of making and using same," ed: Google Patents, 2012.

[25] M. Ozkok, "Direct EP and direct EPAG — Novel surface finishes for gold-, copper wire bonding and soldering applications," in *Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2012 7th International*, 2012, pp. 178-182.

[26] N. Kumbhat, A. Choudhury, M. Raine, G. Mehrotra, P. M. Raj, R. Zhang, *et al.*, "Highly-reliable, 30µm pitch copper interconnects using nano-ACF/NCF," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 1479-1485.

[27] A. Choudhury, N. Kumbhat, P. M. Raj, Z. Rongwei, V. Sundaram, R. Dunne, *et al.*, "Low temperature, low profile, ultra-fine pitch copper-to-copper chip-last embedded-active interconnection technology," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 350-356.

[28] S. A. Khan, N. Kumbhat, A. Goyal, K. Okoshi, P. Raj, G. Meyer-Berg, *et al.*, "High current-carrying and highly-reliable 30μm diameter Cu-Cu area-array interconnections without solder," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 577-582.

[29] K. Maier, "Self-diffusion in copper at “low” temperatures," *physica status solidi (a)*, vol. 44, pp. 567-576, 1977.

[30] P. M. Hall, J. M. Morabito, and N. T. Panousis, "Interdiffusion in the Cu□Au thin film system at 25°C to 250°C," *Thin Solid Films*, vol. 41, pp. 341-361, 1977/03/15 1977.

[31] J. Chakraborty, U. Welzel, and E. J. Mittemeijer, "Mechanisms of interdiffusion in Pd–Cu thin film diffusion couples," *Thin Solid Films*, vol. 518, pp. 2010-2020, 2/1/ 2010.

[32] J. Chakraborty, U. Welzel, and E. J. Mittemeijer, "Interdiffusion, phase formation, and stress development in Cu–Pd thin-film diffusion couples: Interface thermodynamics and mechanisms," *Journal of Applied Physics*, vol. 103, p. 113512, 2008.

[33] J. A. Borders, "Ion back-scattering analysis of interdiffusion in Cu-Au thin films," *Thin Solid Films*, vol. 19, pp. 359-370, 1973/12/17 1973.

[34] L. G. Feinstein and J. B. Bindell, "The failure of aged Cu□Au thin films by Kirkendall porosity," *Thin Solid Films*, vol. 62, pp. 37-47, 1979/09/03 1979.

[35] P. Madakson and J. C. Liu, "Interdiffusion and resistivity of Cu/Au, Cu/Co, Co/Au, and Cu/Co/Au thin films at 25–550 °C," *Journal of Applied Physics*, vol. 68, pp. 2121-2126, 1990.

[36] M. R. Pinnel and J. E. Bennett, "On the formation of the ordered phases CuAu and Cu3Au at a copper/gold planar interface," *Metallurgical Transactions A*, vol. 10, pp. 741-747, 1979.

[37] J. Lohmiller, R. Spolenak, and P. A. Gruber, "Alloy-dependent deformation behavior of highly ductile nanocrystalline AuCu thin films," *Materials Science and Engineering: A*, vol. 595, pp. 235-240, 2/10/ 2014.

[38] L. Xie, S. Wickramanayaka, S. C. Chong, V. N. Sekhar, D. Ismeal, and Y. L. Ye, "6um Pitch High Density Cu-Cu Bonding for 3D IC Stacking," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 2126-2133.

[39] J. Erlebacher, M. J. Aziz, A. Karma, N. Dimitrov, and K. Sieradzki, "Evolution of nanoporosity in dealloying," *Nature*, vol. 410, pp. 450-453, 03/22/print 2001.

[40] K. Sieradzki, N. Dimitrov, D. Movrin, C. McCall, N. Vasiljevic, and J. Erlebacher, "The dealloying critical potential," *Journal of the Electrochemical Society*, vol. 149, pp. B370-B377, 2002.

[41] W. Rasband, "ImageJ: Image processing and analysis in Java," *Astrophysics Source Code Library*, vol. 1, p. 06013, 2012.

[42] C. Mingxian, C. Mingxiang, and L. Sheng, "Low temperature thermocompression bonding based on copper nanostructure for 3D packaging," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1-4.

[43] R. Mao, S. Liang, X. Wang, Q. Yang, and B. Han, "Effect of preparation conditions on morphology and thermal stability of nanoporous copper," *Corrosion Science*, vol. 60, pp. 231-237, 7// 2012.

[44] Y. Heng, Z. Congchun, Y. Zhuoqing, W. Hong, D. Guifu, and Z. Xiaolin, "A Preparation Method of Patterned Nanoporous Copper," *Advanced Materials Research*, vol. 663, pp. 322-325, 2013.

[45] C. Yang, Q. B. Zhang, M. Y. Gao, Y. X. Hua, and C. Y. Xu, "In Situ Electrochemical Fabrication of Three Dimensional Hierarchical Nanoporous Copper Films and Their Electrocatalytic Performance," *Journal of The Electrochemical Society*, vol. 163, pp. D469-D475, January 1, 2016 2016.