Experimental and Theoretical Assessment of Thin Glass Substrate for Low Warpage
Scott McCann, Vanessa Smet, Venky Sundaram, Rao R. Tummala, and Suresh K. Sitaraman

Abstract—This paper compares the warpage after lead-free solder assembly of ultrathin glass and organic substrates for microelectronic packages. Smart mobile devices demand packages to be thinner, which exacerbates warpage, which in turn affects interconnect pitch scaling and reliability. Although low-coefficient-of-thermal-expansion (CTE) organic laminates have been developed to reduce the warpage during assembly, glass substrates offer added benefits of much higher modulus and thermo-mechanical stability, with the potential to reduce warpage beyond low-CTE organic materials. The focus of this paper is on modeling and measurements to quantify the warpage of glass and organic laminates at 100-μm core thickness after thermo-compression bonding at 260 °C peak temperature. In the experiments, four-metal-layer glass substrates were fabricated at the panel level, diced into 18.4 × 18.4-mm² coupons, 10-mm × 10-mm × 630 - μm silicon dies were thermocompression bonded, and the warpage of the assembled packages was measured using shadow moiré interferometry. In parallel to the experiments, numerical models that account for the viscoelastic behavior of the solder as well as the sequential build-up materials and processes have been developed. The predicted warpage from the models was compared to the experimental measurements. It was seen that the low-CTE glass had lower warpage than the organic core of equivalent CTE, while increasing the CTE of the glass increased the warpage. Also, the underfill fillet size was found to influence the warpage for thin substrate packages, and an optimal fillet size has been identified for minimizing warpage. B-staged and capillary underfill materials were compared and found to have similar warpage values.

Index Terms—Die warpage, element birth and death, finite element simulation, substrate warpage, thin glass substrate.

I. INTRODUCTION

 Device packaging today is commonly performed with organic substrate cores such as FR4 or BT on which dry film organic build-up layers are deposited to form wiring layers on both sides. However, organic packaging is limited for future mobile packaging and high performance needs due to the electrical and mechanical properties of the material. For example, the coefficient of thermal expansion (CTE) mismatch between the organic substrate and silicon die creates warpage before and after lead-free solder assembly. The demand for thinner packages for mobile applications imposes stringent requirements for ultrathin substrates, which exacerbates warpage challenges.

One of the single biggest barriers to ultrathin packages is the substrate warpage during chip assembly. The mismatch of CTE between the silicon ICs (3 ppm/°C) and typical organic laminate substrates (12–18 ppm/°C) not only causes warpage during assembly, but also induces stress in the interconnections leading to solder joint failures. Traditional organic laminates such as FR-4 or BT, with prepreg or build-up epoxy dielectric based redistribution layers (RDLs) are the main substrates used for fine-pitch ball grid array (BGA) packages [1], [2]. Such organic substrates are often thick with a core thickness ranging from 500 μm to 1 mm to allow for sufficient rigidity and low warpage to meet the JEDEC standard specifications [3]. Recently, ultralow CTE organic laminates with CTE in the range of 2–6 ppm/°C have been developed to address the warpage challenge, by increasing the filler loading and by changing the glass fabric reinforcement to lower CTE glasses. These low-CTE laminates have significantly improved the warpage control during IC assembly, with a 7.3-μm thick x 7.3-μm x 150-μm silicon chip on a 14-μm x 14-μm x 260-μm package substrate (core CTE of 1.8 ppm/°C), resulting in a warpage of about 70 μm at room temperature and about 35 μm at reflow temperature [4]. Although silicon or ceramic substrates can address the warpage with a combination of low CTE and high elastic modulus, high cost coming from small wafers or substrates has been a major impediment to adoption in smart mobile systems.

Glass is an ideal candidate for next-generation packaging, combining the best electrical properties of ceramics, high dimensional stability of silicon, and large panel processing of organics for low cost [5]. The higher elastic modulus of glass should enable much thinner packages than organics for the same warpage specifications. The CTE of the glass can be tailored, allowing larger glass packages to be directly SMT attached to FR-4 boards with high reliability [6]. Glass is smooth and planar, and, therefore, amenable to fabricating ultraprecise fine lines and spaces [7]–[9]. However, glass does have challenges in handling, brittleness, and through via formation at high speed, although significant progress has already been demonstrated in addressing these challenges [10]–[12]. Although lower warpage is anticipated for glass than organics, given its much higher elastic modulus and low CTE, there has been no published literature quantifying the warpage of low CTE glass and organic substrates during IC assembly.
The objective of this paper, therefore, is to model, design, fabricate, and measure the warpage of glass and organic laminates at 100-µm core thickness after thermo-compression bonding (TCB) at 260 °C peak temperature. A cross-sectional schematic of the proposed glass BGA package for a smart mobile application is seen in Fig. 1. Using detailed finite element modeling (FEM) studies, this paper studies core CTE, core modulus, die and substrate thickness, underfill fillet size, and underfill type. This paper extends beyond the initial studies previously reported [13], which was limited to two metal-layer substrates and simple test designs.

II. GLASS SUBSTRATE FABRICATION AND ASSEMBLY

This section outlines the fabrication process that was carried out to create glass substrates starting with a bare thin glass panel. The panel was a low-CTE EN-A1 glass from Asahi Glass Co. Ltd., measuring 150 mm × 150 mm × 100 µm, and would produce a six-by-six array of 18.4 × 18.4 mm² four-metal-layer substrates. Although the processing was carried out on a panel, for the sake of clarity, the process steps are described using one substrate, as illustrated in Fig. 2.

A. Glass Panel Fabrication

First, a bare glass panel was cleaned and dried, shown in Fig. 2(a). A surface treatment was applied to both sides to enhance the adhesion between the glass and polymer. Then, 17.5-µm polymer layer of ZEONIF ZS-100 was vacuum laminated on both sides of the glass panel using a 60-s vacuum and 10-s pressure. The panel was hot pressed at 115 °C for 90 s, and then the polymer was cured at a temperature of 162 °C for 60 min [Fig. 2(b)].

The polymer-laminated panel was then cleaned using a desmear process. A copper seed layer was then deposited using an electroless bath [Fig. 2(c)]. After the electroless copper is deposited, a dry film photoresist was laminated. A development photoresist from Hitachi was exposed and developed [Fig. 2(d)]. Copper was then electroplated to 10 µm thick, as seen in Fig. 2(e). The photoresist was stripped, and the copper seed layer is etched, leaving one metal layer on each side of the panel [Fig. 2(f)]. This method of copper deposition and patterning is known as semiadditive process (SAP). The above process steps [Fig. 2(b)–(f)] are repeated to create the next metal layers [Fig. 2(g)].

After the final metal layers were fabricated, a dry-film photosensitive solder resist was laminated, cured, exposed, and developed to expose substrate copper pads for flip-chip assembly. An electroless nickel immersion gold surface finish was used on the exposed copper pads.

Although metal layers were present on top and bottom of the glass substrate, no through-glass or polymer vias were fabricated in this paper because through vias are expected to have little effect on warpage. Fabrication and reliability of vias through glass are being pursued by other researchers within the 3-D Packaging Research Center at Georgia Tech [14], [15].

B. Silicon on Glass Interconnect Assembly

Prior to assembly, the 150 × 150 mm² glass panel was diced at 1 mm/s into a six-by-six array of 18.4 × 18.4 mm² using a Disco dicing tool with a blade intended for silicon.

A 10 × 10-mm² 630-µm-thick silicon die was then assembled to the glass substrate, as shown in Fig. 2(h). The silicon die, which was bumped with tin–silver solder, was assembled on the glass substrate by TCB, and the conditions varied based on the type of underfill. For B-staged underfill, which was present during the assembly process, the peak tool head temperature was 280 °C with 50-MPa pressure for 5 s with the stage held at 70 °C. For capillary underfill, which was not present during the assembly process, the peak tool head temperature was 260 °C with 1.5-MPa pressure for 5 s with the stage held at 70 °C (Fig. 3). Additional details on the TCB can be found in [16].

Two different types of underfills with similar modulus and CTE, namely, capillary underfill and B-stage underfill, were used for different test vehicles to investigate the effect of underfill timing on warpage. For the capillary underfill, the underfill was dispensed in an L-shape along two edges of the die, and the underfill flowed under the die through capillary action after TCB. Fillets were added for the remaining two edges of the die after the capillary action, and the underfill was cured at 165 °C for 90 min. For the B-stage underfill, the underfill was dispensed on the die and B-staged for 1 h at 70 °C prior to die assembly and the package was cured at 165 °C for 3 h after assembly. A silicon die assembled on a glass substrate with a B-staged underfill is shown in Fig. 4.
Fig. 3. Tool head temperature and pressure profile used for TCB on capillary underfilled samples. The stage is held at 70 °C throughout the process.

Fig. 4. Silicon die assembled on a four-metal-layer glass substrate with B-staged underfill.

TABLE I
SAMPLES FABRICATED

<table>
<thead>
<tr>
<th>Core Material</th>
<th>Core CTE (ppm/°C)</th>
<th>Underfill</th>
<th>Number of Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-CTE Glass</td>
<td>3.8</td>
<td>B-Staged</td>
<td>2</td>
</tr>
<tr>
<td>High-CTE Glass</td>
<td>9.8</td>
<td>B-Staged</td>
<td>3</td>
</tr>
<tr>
<td>Organic</td>
<td>3.3</td>
<td>B-Staged</td>
<td>3</td>
</tr>
<tr>
<td>Low-CTE Glass</td>
<td>3.8</td>
<td>Capillary</td>
<td>2</td>
</tr>
</tbody>
</table>

III. DIE WARPAGE MEASUREMENTS

Shadow moiré measurements were done using akrometrix’s TherMoiré PS200S to determine the warpage of the die–substrate package. Details on shadow moiré can be found in several publications [17]–[19]. The samples measured for warpage are presented in Table I.

An example shadow moiré collected for the low-CTE glass sample at room temperature over the die region is shown in Fig. 5. The die region measurements were taken from the die side. The warpage values are computed by looking at the maximum and minimum out-of-plane displacements from the shadow moiré experiments. For example, as seen in Fig. 5, the die region has a positive displacement of 3 μm, while the substrate corners have a negative displacement of 5 μm, and thus, the overall warpage for this die–substrate package is 8 μm. The warpage was dome shaped because the substrate contracted more than the die at room temperature.

Die warpage was determined as the difference of the die center height and the average corner height, and thus, the data for each sample at a given temperature are the average of four measured values. Shadow moiré data were collected over a temperature range of 25 °C–260 °C, covering the range of temperatures experiences in a 260 °C reflow cycle, which is necessary to attach the package to a system board. The error margin of the tool and grating used is ±1.5 μm.

It should be pointed out that at temperatures above 220 °C, the solder is likely to be in molten state and, thus, will provide practically no mechanical coupling between the die and the substrate. Therefore, at temperatures close to 220 °C and above, the warpage will be minimal, as seen in Fig. 6.

Fig. 6 shows a comparison of the measured die warpage as a function of temperature for low-CTE glass and low-CTE organic samples. As seen, the die had a maximum warpage at room temperature, and this warpage continued to decrease as the temperature was increased toward the stress-free temperature. The stress-free temperature for the dielectric polymer on the glass substrate was 162 °C, for the solder assembly was 220 °C, and for the underfill cure was 160 °C. Therefore, in general, the die region had less warpage at higher temperature than at room temperature.

These samples had identical CTEs (3.3 ppm/°C). The glass had a modulus of 77 GPa, and the organic had a modulus of 36 GPa. Comparing the low-CTE glass and the low-CTE organic samples (Fig. 6), the higher modulus core of the glass
samples provided greater rigidity to the package, which led to lower warpage.

Fig. 7 shows a comparison of the measured die warpage as a function of temperature for low-CTE glass and high-CTE glass samples. These samples had similar moduli (77 GPa for the low-CTE glass and 74 GPa for the high-CTE glass), but the high-CTE glass had a CTE of 9.8 ppm/°C, while the low-CTE glass had a CTE of 3.3 ppm/°C. Similar to the other samples, high-CTE Glass showed maximum warpage at room temperature, decreasing warpage with increasing temperature, and minimal warpage above 160 °C. Comparing the low-CTE glass and the high-glass samples, low-CTE glass samples have less warpage because there is less CTE mismatch between the substrate and silicon die.

IV. SIMULATION

In parallel to experiments, finite element models were created to understand the role of substrate properties and assembly processes on warpage. The modeling was done parametrically in ANSYS 14.5, using plane-strain approximation.

A. Model Geometry and Mesh

Although 2.5-D or 3-D models are desirable to account for property and geometry variations in the third dimension, 2-D models are appropriate for comparison between different cases. Fig. 8 shows a schematic of the plane-strain model for the low-CTE glass sample. The glass or organic substrate, the polymer layers, copper RDLs, solder interconnects, underfill, and silicon die were included in the models. There were no vias in the models, as in the experiments. The die–substrate assembly was cut along the diagonal with symmetry boundary conditions on one side, as illustrated in Fig. 8. One node at the left bottom was fixed in the y-direction to prevent rigid body motion. The fixed node was within the glass, as the glass is present from the beginning of fabrication, which is important for process modeling.

B. Material Properties

Table II shows the thermo-mechanical material properties used in the models. Silicon’s modulus is directionally dependent based on crystal orientation and standard processing, with the in-plane modulus being higher than the out-of-plane modulus or [100] direction [20]. Properties for the polymer, ZEONIF ZS-100, were obtained from the manufacturer, Zeon Corporation. The low- and high-CTE glass represent the published properties for Asahi Glass Co., Ltd.’s glass [21]. For the electroplated copper, temperature-dependent material properties were used [22]. An Anand viscoplastic model of solder was used to model the deformation of tin–silver solder [23], [24]. No surface finish was simulated as surface finish thickness was several orders of magnitude less than the substrate thickness, and thus, the presence of surface finish in the model was not likely to influence the predicted warpage results.

C. Process Modeling: Element Birth and Death

To mimic the actual fabrication process, element “birth” and “death” were used in the simulation model. At the beginning of process simulation, only the glass core was present, as shown in Fig. 2(a). Therefore, the simulation started with “birthing” the glass panel, and “killing” all other layers or materials. Such a “killing” or death means that such material elements were present in the model, however, with a modulus of elasticity that is six orders of magnitude less than other “birthed” materials.
Material elements were “birthed” sequentially with their actual properties at their stress-free temperature (Table II).

Fig. 9 illustrates the solution steps for a four-metal-layer package. As seen, starting from room temperature: 1) the glass core was simulated to be heated to 160 °C, the temperature at which the dielectric polymer was cured; 2) the glass core and polymer were then simulated to be cooled to room temperature; 3) subsequently simulated to be heated to 40 °C; and 4) the temperature at which copper was electroplated. The process steps were repeated for the next two metal layers (5–9). These simulation steps completed the fabrication of the glass substrate with RDLs.

The next step was to simulate the flip-chip assembly process. The substrate with build-up layers was then simulated to be heated to 220 °C, the melting temperature of tin–silver solder, to mimic the reflow assembly process, where the chip, solder, and chip pads were “birthed” (10). The assembly was then uniformly cooled to the underfill cure temperature of 160 °C (11) and then further cooled down to room temperature (12). This simulation mimics the B-staged underfill cure process. On the other hand, for a capillary underfill, the assembly is first cooled to room temperature from the reflow temperature, underfill is then dispensed at 90 °C on a hot plate, and then the underfill is cured at a temperature of about 160 °C. The current model does not include such cooling and reheating steps, as the results from both modeling approaches are nearly the same [26]. Also, the current single-step cooling model from reflow temperature to room temperature through underfill cure temperature is less computationally expensive. Thus, the warpage of the assembly through the entire fabrication and assembly process simulation is captured.

D. Warpage Prediction and Validation

The warpage predicted by the finite element models was validated against warpage measured using shadow moiré. An example of this validation is depicted in Fig. 10, which shows the two experimental samples and simulated warpage data as a function of temperature for the low-CTE glass sample. Both experimental and simulated results show the maximum warpage at room temperature, and the magnitude predicted by the simulations agrees with the experimental data. The model captures the decrease in warpage as the temperature is increased.

Through vias were not included in the experimental samples and the corresponding modeling because they were expected to have relatively little effect. Models with fully filled through vias were constructed to investigate the validity of this claim. Except for the presence of the vias, the models were otherwise identical to low-CTE glass samples in Table I. Assuming 100-µm-diameter vias in an 18.4 × 18.4-mm² substrate with 400-µm board-level pitch on, the maximum necessary total copper volume is less than 5%. With this number of vias, the warpage increases by 8.8% compared to the case without vias. However, the typical number of vias is often much lower, at 1% or less. With this number of vias, the warpage increases by 0.3% compared to the case without vias.

E. Effect of Die and Substrate Thickness

The warpage depends on both the die and substrate thickness as seen in Fig. 11, in which the predicted die warpage for 100-, 200-, 400-, and 630-µm dies is plotted for 50-, 100-, 200-, 300-, 400-, 500-, and 600-µm-thick glass substrates at 25 °C. The structures are otherwise assumed to be identical to the low-CTE glass samples in Table I. From this plot, decreasing the die thickness increases the warpage. Also, decreasing the glass thickness increases the warpage. However, as long as the overall package is at 400-µm thick, the die warpage is not predicted to exceed 10 µm. JEDEC requires warpage to be less than 100 µm [3]. A package that is 400 µm thick, includes 70 µm of dielectric polymer, 40 µm of copper, and a 10 × 10-mm² die, and exhibits less than 10 µm warpage (Fig. 11) shows glass is a strong candidate for low warpage.

V. UNDERFILL FILLET

Package-level warpage is important for board-level assembly, and thus, substrate warpage is modeled and experimentally
characterized. Fig. 12 shows an example shadow moiré measurement of the substrate at room temperature for a low-CTE glass sample. Substrate warpage measurements are taken from the non-die side due to the step height limitation of the shadow moiré technique.

It was observed that the die and substrate warp in different directions below the stress-free temperature, as seen in Figs. 5 and 12. This was because of the underfill fillet. As the underfill used in our study has a large CTE, it shrinks more than the surrounding material, exerting a force that causes the substrate to bend. Thus, substrate warpage is influenced by the underfill fillet. Fig. 13 shows a cross-sectional schematic of this effect at room temperature. Near the stress-free temperature, the package is flat because the underfill fillet exerts no force on the package.

With no underfill fillet or a very small fillet, the substrate continues the dome shape of the die region below the stress-free temperature, as shown in Fig. 13(b). At the stress-free temperature, the substrate is near flat. Varying the fillet size between large [such as in Fig. 13(a)] and very small [such as in Fig. 13(b)] varies the amount of substrate warpage, and an intermediate size fillet is shown in Fig. 13(c).

A. Experimental Substrate Warpage

Shadow moiré measurements for substrate warpage, such as in Fig. 12, were taken over a range of temperatures, and the results are shown in Fig. 14 for low-CTE glass samples. Fig. 14 also includes the finite element model prediction. The finite element model used a fillet size of 240 µm to track the experimental data. At 25 °C, the model predicts a shape that is dome-like where the die is and bowl-like beyond the die region, similar to the W-shape in Fig. 13(a). As seen, the simulations show decreasing warpage with increasing temperature. The warpage is minimum near the underfill cure temperature. This is to be expected because the large structures in the assembly, namely, the die and the substrate, are tightly bonded together by the underfill at the underfill cure glass transition temperature, and thus the underfill cure temperature is near the stress-free temperature for the assembly.

B. Effect of Underfill Fillet on Substrate Warpage

The warpage is influenced significantly by underfill fillet, and along a die edge, there was a continuous fillet that
Fig. 15. Warpage (µm) contour plot of low-CTE glass samples (Table I) with (a) full fillet, (b) half fillet, and (c) no fillet, at 25 °C.

influences the substrate warpage. This fillet can be adequately captured through plane-strain approximation. On the other hand, the corner warpage is influenced by the fillets on both edges of the corner as well as the corner fillet itself, and therefore, it is difficult to capture through one cross-section model. The simulation result shown in Fig. 14 assumes a 240-µm fillet to match the experimental data. For a fillet that is 630 µm tall (touches the top edge of the die) and 630 µm long, the deformed assembly images are shown at 25 °C in Fig. 15(a). This result is similar to the shape seen in Fig. 13(a).

To understand the role of the underfill fillet size, different sizes of fillets were simulated. In all of the simulations, the stress-free temperatures, the geometry, and the mesh were kept identical to be able to compare different cases. The warped geometry, as simulated, with a fillet that is 315 µm tall and 315 µm long is shown in Fig. 15(b) at 25 °C. As seen, the substrate was less warped than the full fillet [Fig. 15(a)]. The third case, which has no fillet, was also simulated, and the results are shown in Fig. 15(c). The no fillet case is nearly flat. In all cases, the die warpage is nearly identical, and this is because the fillet has minimal effect on the warpage of the die.

The substrate warpage is relevant in package to board assembly, and the planarity of the package determines whether assembly is feasible. As the substrate warpage is a function of the fillet size, it is possible to optimize the fillet size for a minimum substrate warpage. For the low-CTE glass samples (Table I), the model predicted a minimum substrate warpage with an 81-µm fillet. It should be noted that the optimal fillet size will change as a function of sample geometry, material CTE, and material modulus.

The degree to which the influence of the underfill fillet is observed is enhanced by how thin the glass substrate is and how thick the silicon die is. The impact of underfill fillet size observed in glass should be true for other similarly thin substrates as well.

C. Capillary and B-Staged Underfill Comparison

Low-CTE glass samples with capillary underfill were fabricated in addition to low-CTE glass samples with B-staged underfill to compare underfill materials. Fig. 16 shows the comparison of die warpage measured using shadow moiré. The die warpage results are similar between the two underfills, indicating that the two underfills couple the die and substrate together to a very similar degree. This is because the modulus of the two underfills is very close, at 2.9 GPa for the B-staged underfill and 3.0 GPa for the capillary underfill. Based on these data, the underfill type has little impact on the warpage and the choice for underfill will be based on other considerations, such as desired bump pitch and assembly process conditions.

VI. CONCLUSION

The objective of this paper is to develop a flip-chip package with low warpage and understand the role of various parameters on warpage.

This paper has experimentally used thin glass panels as the core material for microelectronic packaging and found to have low warpage due to the high rigidity and silicon matched CTE of glass. The fabrication process to deposit build-up materials creates residual stresses due to the CTE mismatch between the core and build-up materials. This paper employed similar structures on both sides of the glass panel, resulting in minimal warpage prior to assembly. The die is thermo-compression bonded and warpage is measured from the die and substrate sides. Low-CTE glass was demonstrated to have lower die warpage than low-CTE organic because it has a higher modulus, providing greater structural rigidity. Low-CTE glass also had lower warpage than high-CTE glass because it has less CTE mismatch with the silicon die. These warpage values are all lower than what is required by the JEDEC standard.

In conjunction with the experimental work, physics-based finite element models have been developed to mimic fabrication and assembly processes. The model predictions agree well with the warpage values and trends seen from experiments. The underfill fillet greatly influences the shape of the substrate warpage after assembly at room temperature. Larger fillets warp the substrate upward around the die, while smaller fillets have less impact on the substrate warpage. It is possible to minimize substrate warpage through fillet size control, and an optimal fillet size for minimum warpage was identified.

ACKNOWLEDGMENT

The authors would like to thank M. Kobayashi, A. Mieno, S. Raghavan, C. White, and J. Bishop.
REFERENCES


