Design and Demonstration of Highly Miniaturized, Low Cost Panel Level Glass Package for MEMS Sensors

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***Abstract* — This paper describes an ultra-thin, low cost 3D glass sensor packaging platform for near-hermeticity with novel feedthrough and encapsulation technologies. Glass panels of thicknesses ranging from 50 µm to 300 µm are used which limits overall form factor to <0.7 mm. A process flow for fabrication of cavity/embedded sensor packages is described with demonstration three unique fundamental technologies. Vertical electrical feedthroughs are demonstrated using a low-cost conductive Transient Liquid Phase Sintering (TLPS) paste in a high throughput process. Lateral electrical feedthroughs embedded in polymer trenches are proposed for higher reliability, better coplanarity, reduced vulnerability to chemical corrosion and lower parasitics. Finally, four different adhesive polymers are explored to demonstrate a low temperature glass-glass panel bonding technique. Samples bonded at fixed conditions using the four polymers showed sufficiently high bond strength (>10 MPa) and Dow Chemical's Benzocyclobutene (BCB) 14-P005 is found to be the best candidate for panel level glass-glass bonding. Modelling of the proposed three-layer glass packaging platform was performed in COMSOL Multiphysics. Results show a maximum deformation of about 2.3 µm - 2.5 µm in the BCB and GX-92 bonded package and the least average internal stress of 6.40 MPa in the BCB bonded package. The complete manufacturing cycle starting from cavity formation on bare glass to final 3D assembly to form the lidded/open cavity package including singulation is panel based, enabling significant cost reduction (depending on die dimensions and panel size) compared to ceramic and other substrate technologies.**

Keywords – glass; MEMS; sensors; package; panel; cost; hermeticity; feedthrough; bonding

I. INTRODUCTION

MEMS and sensing electronics has been a rapidly evolving industry since the early 2000s [1]. The meteoric rise of the Internet of Things (IoT) market has proven to be the main driver toward the deployment of billions of sensors in countless applications across various domains. The smart phone and medical electronics market is booming with demands for higher functionality, biocompatibility, efficient powering, small size, low cost and high volume manufacturability (HVM). Automotives, in particular is a promising market for the electronics industry with the most diverse needs. Advanced Driver Assistance Systems (ADAS) and passenger safety systems use pressure sensors, image sensors, LIDAR, and RADAR while Air Quality Maintenance (AQM) systems employ gas and temperature sensors to monitor cabin air quality. These technologies are aimed at making driving safer and more comfortable.

With such an increased proliferation of sensors in different markets, the importance of size reduction, cost-effectiveness, high performance, low power consumption, heterogeneous integration and high reliability by means of advanced packaging is at its peak. However, despite critical functions like mechanical protection, power delivery, signal redistribution, environmental access and thermal management, packaging adds no value to the system by itself. In fact, it takes up the largest fraction of overall manufacturing cost [2]. In most applications like environment monitoring (temperature, gas concentration, humidity, and pressure), gyroscopes and image sensors, either over-molded packaging with BGA or ceramic, metal, laminate and rigid/flexible polymer cavity packages are used in combination with wire-bond/flip-chip interconnection technology. Ceramic packages are reliable, chemically resistant, easy to machine and have enabled integration of multiple sensors by means of high density interconnections between chip and substrate [3]. However, they are not suitable for miniaturization due to their thickness. Metal packages provide efficient thermal management and EMI shielding and are widely used to package sensors used in harsh environments but are restricted to low volume manufacturing. Moreover, despite showing good hermeticity, metals and ceramics are also significantly more expensive compared to plastic packages [4]. Polymer packages, while

being low cost, are non-hermetic and show poor reliability due to large CTE mismatch with the silicon based devices.

Literature related to standardized MEMS packaging techniques is scarce since most techniques are application specific, non-commercialized and therefore remain proprietary [5]. Each MEMS package comes with a unique set of challenges like poor mechanical strength, lack of physical protection, contamination and non-hermetic sealing [4]. Therefore, despite showing good performance and sensor integration capabilities, the challenge and research focus for MEMS and sensor packaging is to meet all performance and reliability criteria while furthering miniaturization and keeping manufacturing cost low by employing high yield wafer/panel level manufacturing technologies. Table I below shows the most recent and widely prevalent packaging technologies implemented toward different applications.

TABLE I. PREVALENT PACKAGING TECHNOLOGIES

Application	Packaging technology
RF MEMS	Glass substrate, silicon cap
Image sensors	Ceramic & polymer substrate, glass cap
Biosensors	Ceramic & glass hermetic package
Inertial	Ceramic/laminate/polymer package
Environmental	Ceramic, laminate, metal open cavity package

Georgia Tech's Packaging Research Center proposes a novel standardized approach for MEMS/sensor packaging. Using ultra-thin glass as the base, MEMS and sensors are embedded in lidded/open cavities in a sequential panel-level assembly process for high throughput, higher productivity per substrate and depending on panel size, at lowest cost. This packaging technology is applicable to biosensors, electrochemical sensors, pressure sensors, image sensors and RADAR modules for automotive vision systems and suitable for integration with source data processing and data fusion for various market domains.

The principal topics of discussion in this paper are: (i) process flow for panel glass sensor packaging platform, (ii) novel horizontal and vertical hermetic feedthrough technologies, (iii) Glass-glass low-temperature adhesive bonding for near-hermetic applications and (iv) review of glass cavity formation methods. Additionally, Multiphysics COMSOL results of modelling stress in the adhesive bond that help in optimization of the package design are presented. Section II describes proposed package designs and process flows, section III sheds light on fundamental manufacturing technologies involved and section IV shows results of COMSOL modelling. Finally, conclusions are drawn in section V.

II. GLASS PACKAGING PLATFORM

As a MEMS/sensor packaging material, glass has been used for a long time. Glass substrates with silicon/SOI caps [6, 7] have been commonly used for hermetic sealing of inertial MEMS devices whereas the implementation of silicon/SOI substrate based MEMS structures sealed with glass caps have also been previously demonstrated for harsh oceanic environments [8] and implantable neuromuscular stimulators [9]. Silicon substrate bonding to silicon cavity is very common for sealing of RF MEMS. Unique, application specific packaging techniques, like glass-in-silicon capping layer bonded to an SOI MEMS wafer for packaging of resonators [10] have been demonstrated as well.

In this paper, an all-glass packaging platform is proposed. Table II below lists the properties of glass compared to metals and ceramics. Smooth surface finish, superior electrical performance, inertness, low cost, possibility of high density I/Os, non-hygroscopy, mechanical robustness and Si-matched CTE make glass an ideal candidate for MEMS and sensor packaging.

TABLE II. PROPERTIES OF GLASS FOR USE AS PACKAGING PLATFORM

Parameter	Ideal Properties	Materials		
		Glass	Metal	Ceramic
Electrical	High Resistivity			
	Low Parasitics			
Physical	Smooth surface finish			
	Large area availability			
	Ultra-thin			
Thermal	High thermal conductivity			
	Si-matched CTE			
Mechanical	High strength			
	High modulus			
Chemical	Resistance to chemicals			
Large area processability	Low cost via formation and metallization			
Cost/mm^2	Low cost per I/O at 25 µm pitch			

Good	Fair	Poor

A. *Package Design*

The glass packaging platform involves three main components: (a) Base layer, (b) Cavity layer and (c) optional glass lid/cover glass layer. The base layer acts as a carrier for the MEMS/sensing element assembled by wire bonding or flip-chip assembly. Double sided assembly of sensor/processor allows localized computing and therefore forms a strong case for hetero-integration. The cavity panel forms the cavity for embedding the sensor. Vertical and lateral feedthroughs that allow external access to the device are incorporated in the base/cavity layer. Finally, the cover glass seals the cavity. The proposed packaging platforms are shown in Figure 1.

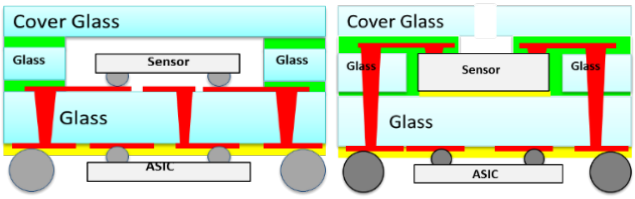

Figure 1. Cavity package and embedded sensor package design

Table III lists the challenges and the research tasks to address and mitigate the challenges expected in realizing the multilayer glass packaging platform.

TABLE III. RESEARCH OBJECTIVES, CHALLENGES AND TASKS

Objectives	Challenge	Research tasks
Low Cost	Yield	Optimize fabrication and assembly for panel level processing
Miniaturization	Thin glass handling, warpage	Low temperature bonding
Reliability	Stress mitigation, bond strength degradation and thermomechanical integrity	Glass bonding for low stress, high bond strength and near-hermeticity. Thermal low stress via design

B. Process Flow

This section describes the process flow for the fabrication of the packaging platform described above. Glass panels measuring 4x4/6x6 inches, commercially available from Corning Inc., Asahi Glass Company and Schott Glass with thickness ranging from of 50µm-300µm can be used. There are two proposed approaches: chip-last cavity package and chip-first embedded-sensor package. Finally, singulation of the panel into discrete chip scale packages is enabled by the dicing tool from DISCO Corporation installed at Georgia Tech.

1) Cavity Package

Base layer fabrication is the first step towards fabricating a cavity package. Vias for vertical feedthroughs are either drilled on laminated glass or pre-drilled on bare glass. Via formation is followed by via filling to form the electrical interconnection. Metallization for lateral feedthrough and metal pads completes the base layer fabrication. Next, the cavity layer is bonded onto the base layer. Finally, after chip assembly, a cover glass is bonded to close the cavity. Figure 2 shows the process flow as described above.

2) Embedded sensor package

The fabrication process for an embedded package involves the same fundamental technologies as the cavity package. A cavity layer is bonded onto a base glass substrate acting as a carrier, after which the MEMS/sensor die is assembled. Vertical and lateral feedthroughs are then fabricated on multiple polymer layers to redistribute the sensor signals externally. Figure 3 shows the process flow for embedded sensor package fabrication where the combination of a peripheral array of vertical feedthroughs and metallization for lateral feedthroughs are fabricated after sensor assembly.

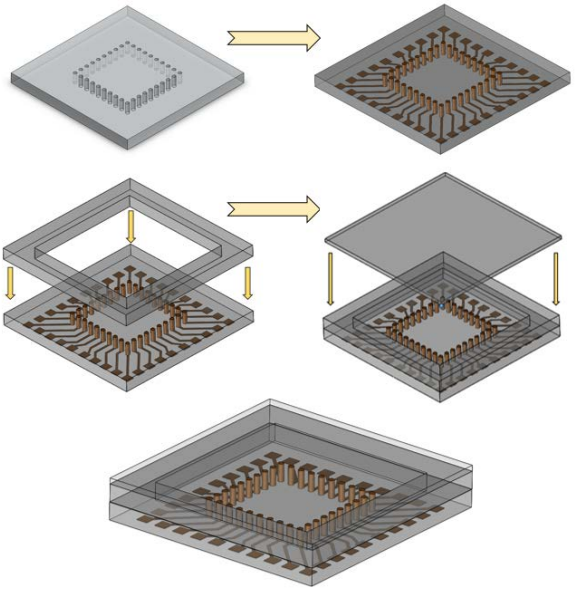

Figure 2. Process flow for cavity package

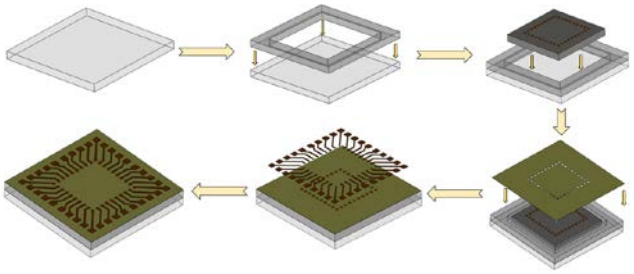

Figure 3. Process flow for embedded package

III. FUNDAMENTAL TECHNOLOGIES

This section discusses three basic technologies used towards fabrication of the glass packaging platform: (a) vertical feedthroughs, (b) lateral feedthroughs and (c) glass-glass panel level adhesive bonding process with characterization of bond strength, followed by a brief review of standard glass micromachining techniques for glass cavity formation.

A. High density vertical feedthroughs

An important component of MEMS sensor packaging is simple, low cost and hermetic feedthrough technologies that show good electrical, thermal and mechanical performance when integrated with the system. Vertical feedthroughs preserve package area, offer lower electrical resistance due to their shorter length and eliminate process complexity involved with non-coplanar lateral feedthrough lines during panel bonding. They also make the package SMT-compatible. Vertical feedthroughs for ceramics have been realized by sintered Pt-paste filled through-vias to connect multiple substrates. However, shrinkage of ceramics poses an issue at the sintering step [11]. Similarly,

gold-sputtered, wet-etched vertical feedthroughs in glass have been demonstrated. Wet etching is a cheap microfabrication solution but forms results in structures with a poor aspect ratio and cannot be used to create high-density vertical feedthroughs. On the other hand, gold is an inert metal and can be used in chemically harsh environments, but like platinum, remains an expensive option [12]. Silicon feedthroughs [6], though highly doped, are still highly resistive compared to metal interconnects which could pose problems in RF-MEMS applications. Silicon feedthroughs in glass using the glass-reflow process offers low throughput cause of its high reflow time of >8 hours, despite offering near-zero parasitic capacitance [10]. Two methods to realize low cost, conductive high-density vertical feedthroughs are described: (a) Metal plating and (b) Conductive metal paste filling.

1) Standard metal plating for via filling

Using established metal deposition methods like electroplating can be used to form hermetic vertical feedthroughs that are simple and inexpensive to fabricate. Reliable, fine pitch vertical interconnections on ultra-thin bare glass using low-resistance copper have already been demonstrated [13, 14] while effects of intrinsic via taper on parasitics has also been extensively studied [15-17]. Therefore, by optimal electrical and thermomechanical design of the vertical feedthrough, losses due to parasitics can be minimized for high signal and power integrity to and from the sensing element while also ensuring high reliability.

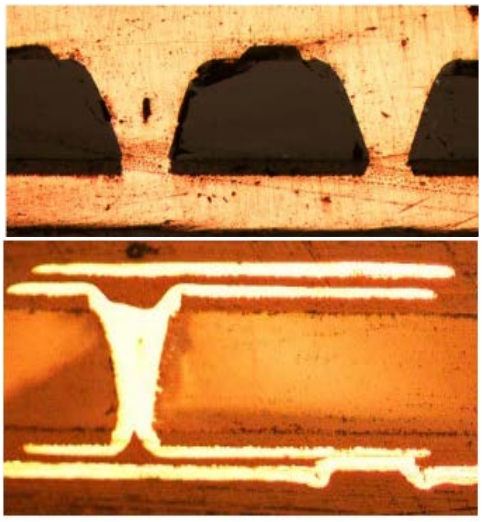

Figure 4. Reliable Cu-plated vertical feedthroughs [18]

2) Low cost, conductive Transient Liquid Phase Sintered paste

A novel conductive sintered paste filling process for near hermetic vertical feedthroughs is described and demonstrated. An electrically conductive sintered paste of copper and tin alloy mixed with flux in a ratio of 97% to 3% by weight, supplied by EMD Performance Materials, is used. The paste is traditionally used as a z-interconnect material in PCBs but due to its favorable properties like low cost, processability, high throughput by screen printing and near-hermeticity has extended its potential for use to package level applications where high density, high aspect ratio interconnects are needed. Importantly, its thermal, mechanical and electrical properties are comparable to those of solders.

Deposition of paste in vias must be preceded by a via-cleaning step. Polymer lamination on glass with vias results in their partial or complete blocking, eventually creating electrical opens. ESI's Cornerstone UV Laser tool installed at Georgia Tech was used for this step. However, since BCB is transparent, it is difficult to confirm whether the polymer is successfully lased away from the via. After multiple attempts with different power values (3W-8W) and various raster settings, the vias were successfully cleaned. Next, the paste was screen printed under the influence of vacuum using a simple stencil. Finally, the paste was sintered in an inert environment between 180^{o} C and 217^{o} C resulting in a continuous metallic joint.

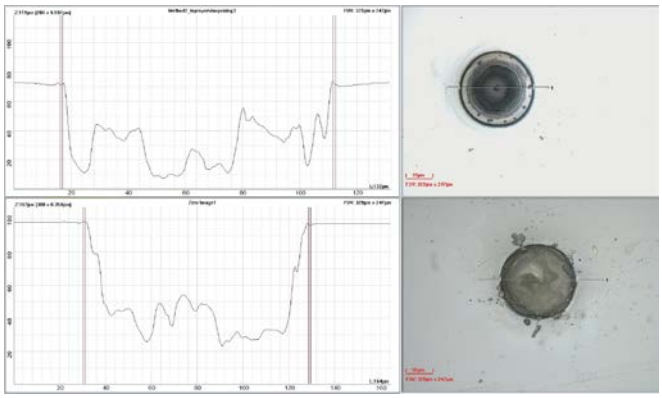

Figure 5. Polymer residues in vias before (top) and after (above) lasing step

Eight test structures with two vias each were fabricated in 300 µm glass. These test structures showed low resistance values ranging from approximately 9Ω - 40Ω compared to 150Ω - 200Ω observed in doped silicon feedthroughs [6]. Three structures showed abnormally high resistance values, which could be due to residual polymer in the vias. The test structure is shown in Figure 6 below.

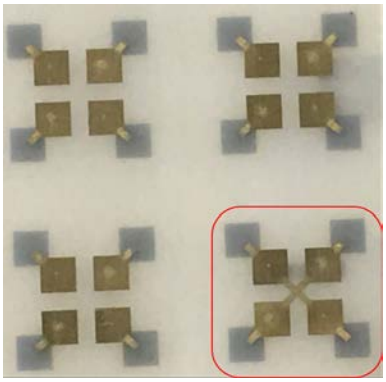

Figure 6. Test structure with 2 paste filled vias, boxed in red

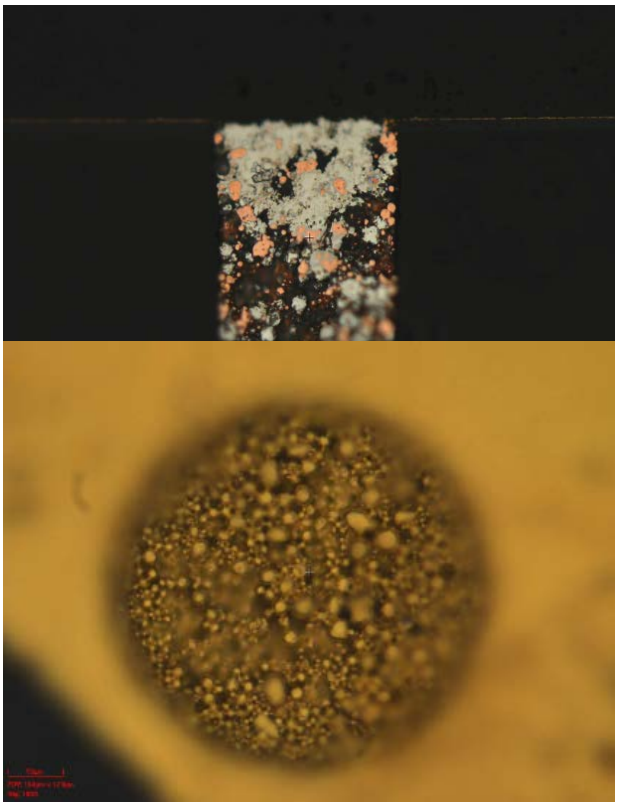

Figure 7. Cross section and top view of paste filled vias

B. *Horizontal feedthroughs*

Buried polysilicon conductors with passivation [9], buried silicon conductors [19] and Aluminum CPWs [20] buried in MEMS wafers are some of the commonly used lateral feedthrough technologies. These, however, face many issues like large electrical parasitics, leakage due to non-coplanarity and chemical corrosion due to non-hermeticity. Most of these solutions are application specific and involve complex fabrication. A low cost, standardized lateral feedthrough technology is required for high reliability, low parasitics, low cost and panel processability.

An embedded trace approach for lateral feedthroughs addressing several concerns is presented. Compared to traditional buried lateral feedthroughs that require deposition of multiple passivation layers, this approach involves trench formation in thin film polymers followed by copper electroplating. Since only the top surface of the metal trace is exposed, the risk of chemical corrosion is reduced. Next, electrical isolation from three sides greatly enhances electrical performance. Finally, higher degree of co-planarity can be achieved by wet etching or cutting overburdened copper to achieve smooth surfaces. An additional polymer layer, due to its flow-ability also provides co-planarity by flowing into micro-cracks. Bonding thin glass with its own redistribution circuitry to form near-hermetic buried lateral feedthroughs is another possibility. The resulting higher co-planarity ensures zero air-gaps after sealing of cavity. In depth information about the embedded trace approach can be found in [21, 22].

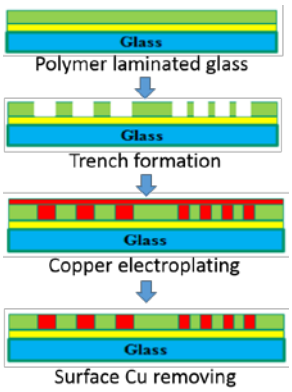

Figure 8. Buried lateral feedthroughs by embedded trench approach [22]

C. *Glass to glass panel scale bonding*

Adhesive wafer bonding uses polymer adhesives as the bonding interface materials (BIM). Compared to fusion bonding, anodic bonding, metal eutectic bonding and thermocompression bonding, adhesive bonding has some significant advantages such as lower cost, high yield, stress buffering, wide applicability to various wafer materials, good adaptability to surface topography, relatively low bonding temperature without the need of electric voltage or current, and compatibility with CMOS as well as MEMS. Adhesive bonding is also a highly parallelized panel-level compatible process, like anodic bonding [23, 24].

Bonding of silicon-silicon and silicon-glass and glass-glass substrates has been extensively studied. Specifically, adhesive bonding using a range of polymers like BCB, SU8 PR, S1818 [23-28] has also been explored, but at high temperatures with limited efficiency. Table IV shows a summary of some of the bonding technologies currently used for MEMS wafer level packaging.

TABLE IV. BONDING TECHNOLOGIES

Bonding Technology	**Substrates**	**Bonding Conditions**
Anodic/field assisted bonding	Si-Si/Si-glass	180ºC - 500 ºC; 200 - 1500V
Direct/Fusion Bonding	Si-Si & glass-glass	600 ºC - 1200 ºC
Eutectic Bonding	Si-Si/Si-glass	200 ºC - 400 ºC Melting point of alloy
Glass frit bonding	Si-glass/glass-glass	< 400 ºC – 1100 ºC
Adhesive Bonding	Si-Si/Si-glass/glass-glass	< 450 ºC

For this study, four different adhesive polymers were explored: BCB, ABF GX92, ABF GY11 (both from Ajinomoto Fine-Techno Co.) and PermiNex 2000 from MicroChem. ABF and BCB are typically used for a variety of reasons like multilayer RDL fabrication and critically, for better handling of glass. Therefore, by testing the adhesive properties of these thin film dielectric materials, the need to use additional adhesive materials is avoided which reduces the number of process steps, temperature cycling and form factor.

TABLE V. LAMINATION PROCESS STEPS

Process step	Process parameters			
	BCB dry film	**GX-92**	**GY-11**	**PermiNex 2000**
Glass cleaning	Standard glass panel cleaning process for cleaning organic residues			
Heating	Bake moisture off the glass			
Adhesion Promoter	O_2 plasma – 10 mins + (DOW Chemical's AP3000/AP9000) 2000 rpm for 45 seconds	O_2 plasma – 10 mins + Silane treatment – 20 minutes @ 70° C		-
Soft bake	120°C for 5 minutes	-	-	-
Lamination	90 °C @ 0.6 MPa; Vacuum dwell for 90s, Pressure dwell for 30s	90 °C @ 0.3 MPa; Vacuum dwell for 90s, Pressure dwell for 30s	90 °C @ 0.3 MPa; Vacuum dwell for 90s, Pressure dwell for 30s	3000 rpm for >30s followed by soft bake @95°C for 5 mins
Bonding				
Oven curing	230°C for 1 hour/250°C for 10 mins followed by ramp down	180 °C for 30 mins	100°C for 30 mins + 130 °C for 30 mins	180 °C for 60 mins

TABLE VI. BONDING METHOD AND ASSOCIATED BOND STRENGTH VALUES

Bonding technique	**Adherent substrates**	**Bond strength with references**
Anodic	Glass-Si	30-40 MPa [29]; >10 MPa [30]
	Si-Glass-Si	>30 MPa [31]; 9.2-10 MPa [32]
	Glass-aluminum	>12 MPa [31]
Fusion	Si-Si	23.5 MPa [33]
Direct	Glass-Glass	10 MPa [34]
Eutectic	Si-gold	18 MPa [35]
Patterned Adhesive	SU-8 to SU-8	16 MPa [27]; 20.6 MPa [28]
	BCB	9-11 MPa [23]

For BCB, GX92 and GY11, a standard lamination process involving glass cleaning, plasma treatment and application of appropriate adhesion promoter by followed by lamination of film is carried out. PermiNex 2000 is spin coated at appropriate values of angular velocity and time followed by a soft bake. The detailed lamination process for each is described in Table V. Microscopic glass slides were used as the base on which 300 um thick glass chips measuring ¼ x ¼ inch were placed centrally and bonded at a relatively low temperature. Using a simple die shear test, bond strength for different adhesives were characterized. Table VI shows the bond strength values previously reported using various bonding methods and Table VII shows preliminary results of the bond shear strength test performed on the samples.

TABLE VII. BOND STRENGTH CHARACTERIZATION RESULTS

Adhesive Polymer	**No. of samples**	**Average bond strength**
BCB dry film	7	> 18.4 MPa
ABF GX-92	4	>18.1 MPa
ABF GY-11	6	13.5 MPa
PermiNex 2000	4	15.7 MPa

All four polymers used for bonding crossed the 10 MPa mark for bond strength, with a minimum of 13.47 MPa and a maximum of about 18 MPa. Bond strength values for BCB and GX-92 are expected to be higher than the ones reported in this paper as substrate failure in some samples as opposed to adhesion failure prevented accurate characterization. Even so, BCB shows the strongest bond, almost twice the 9-11 MPa range reported in [23]. Moreover, other excellent properties of BCB such as good chemical resistance, low gas release, good thermal stability, photosensitivity for area selective bonding, ease of etching and outstanding dielectric properties [24] make it the strongest candidate for panel level glass-glass bonding amongst the four adhesives explored. Being optically transparent, alignment of base and cavity layers is also facilitated. Lastly, the liquid-like behavior of BCB at elevated temperatures makes the sealing of cavities with protruding signal feedthroughs rather straightforward, making the use of embedded feedthroughs unnecessary.

D. Cavity formation

Cavity formation in glass can be accomplished by well-established glass micromachining techniques like wet etching, mechanical etching, DRIE. Extensive literature is published describing these methods in detail [36-42] . Table VIII summarizes the advantages and disadvantages associated with each technique.

For the demonstration of cavity package and embedded sensor package, high quality cavities, shown in Figure 9 and 10 below, were formed by Micron Laser Technology in 300 µm thin glass using a UV laser while Schott Glass provided pre-drilled cavity panels.

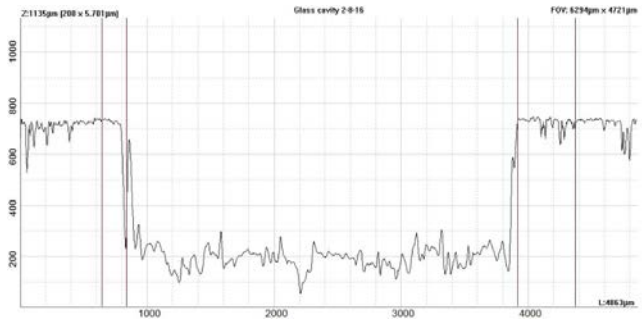

Figure 9. Laser drilled cavity profile

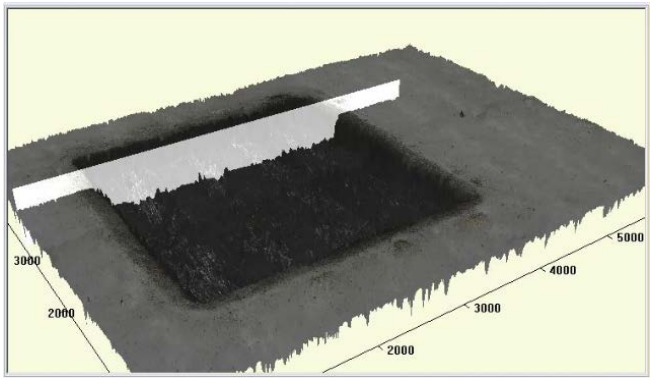

Figure 10. Laser drilled cavity profile 3D view

TABLE VIII. GLASS CAVITY FORMATION METHODS

Approach	Disadvantages	Advantages
Wet Etch	Isotropic etch, low aspect ratio, long time	Cheap, smooth surfaces
Sandblasting	Rough surfaces, tapered profile, low resolution, low selectivity, surface contamination, limit on small features	Simple, low cost, directional ablation
RIE	Process complexity, highly selective mask needed	Good aspect ratio, vertical walls

IV. STRESS DISTRIBUTION

This section describes the modelling of the proposed packaging platform to study its response to thermal cycling. Modelling is done for two purposes: (a) Prediction of stress point locations across the structure and (b) Prediction of package warpage. Based on the modelling results parameters like package dimensions, stack-up and bonding process conditions can be optimized for warpage mitigation, reduced interfacial and bulk stresses across the polymer layer and overall reliability of the platform. Therefore, a model was set up in COMSOL Multiphysics and successive glass panels (base, cavity and lid) bonded with 15 µm thin ABF GX92, ABF GY-11 and BCB adhesives. The base layer measured (5x5x0.3) mm; the cavity layer also measured (5x5x0.3) mm with a cavity opening of (4x4) mm; and the cover glass measured (5x5x0.1) mm. Mechanical properties of each polymer are shown in Table IX below.

TABLE IX. PROPERTIES OF POLYMERS USED IN COMSOL MODELLING

Material	Young's Modulus [GPa]	CTE [10^{-6} K^{-1}]	Thermal Conductivity [W/(mK)]
ABF GX92	5	39	0.15
ABF GY11	8.9	26	0.15
BCB dry film	2.9	42	0.29

Being a simple, preliminary study, the model was run under ambitious assumptions: (a) Bonding temperature is 105° C, (b) Stress and deformation at bonding temperature is zero, (c) linear elastic model. Temperature was ramped down from 105° C to room temperature and initial warpage-induced stresses were computed. Table X shows the values of the stresses.

TABLE X. MODELLING RESULTS

Adhesive	Maximum stress	Minimum stress	Volume-average stress	Maximum deformation
BCB	25 MPa	53 kPa	6.4 MPa	2.32 µm
ABF GX-92	39 MPa	82 kPa	9.6 MPa	2.51 µm
ABF GY-11	43 MPa	93 kPa	11 MPa	1.92 µm

Figure 11, 12 and 13 show the distribution of stresses across a section of the BCB, ABF GX-92 and ABF GY-11 bonded cavity packages. Maximum stresses for all 3 cases are seen at the four corners of the structure at the polymer glass interface.

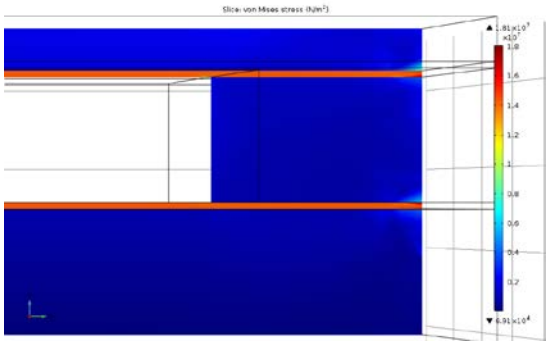

Figure 11. Stress distribution in BCB-bonded cavity package

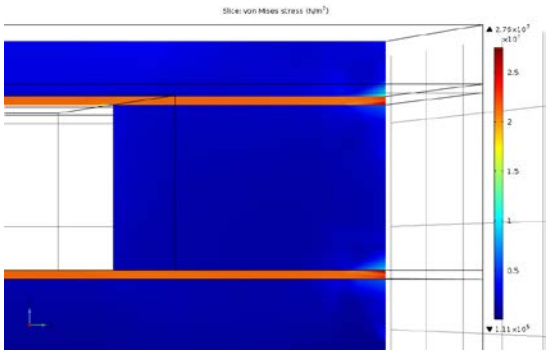

Figure 12. Stress distribution in GX-92-bonded cavity package

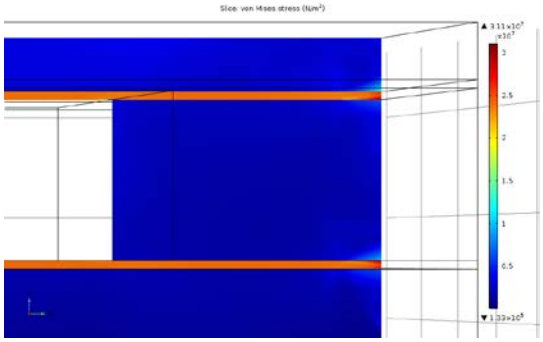

Figure 13. Stress distribution in GY-11-bonded cavity package

Figure 14 shows the maximum deformation caused due to the temperature cycling on each of the three modelled stack-ups representing the warpage along the diagonal.

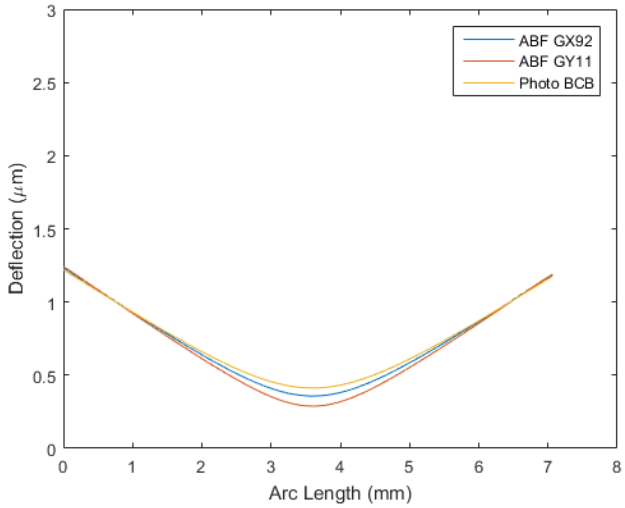

Figure 14. Maximum package deformation along diagonal measuring 7.07 mm

It can be inferred from the modelling results that the stress at the corners of the cavity package exceeds the experimental bond strength values which could cause corner delamination and eventual bond failure over multiple thermal cycles. Accurate, robust modelling for optimization of package design and fabrication is necessary to help create a more reliable packaging platform.

V. Conclusions

This paper explains the process flows for the fabrication of a cavity package and embedded sensor package platform, shown in Figure 15 and 16 and describes three basic technologies used towards fabricating the platform: (a) a novel low temperature glass panel bonding method where BCB was shown to be the best candidate as the adhesive, (b) low cost sintered paste via-filling for vertical feedthroughs and (c) embedded copper traces for lateral feedthroughs. The overall feasibility of glass panel packaging in terms of response to temperature change is also studied for the cavity package. Future work being pursued in this domain by the authors includes testing the feasibility of thin glass (<100 μm) and large panels for high volume manufacturability, detailed stress modelling with higher accuracy, reliability studies with failure analysis of the fundamental technologies discussed and hermeticity tests for the completed cavity and embedded sensor package.

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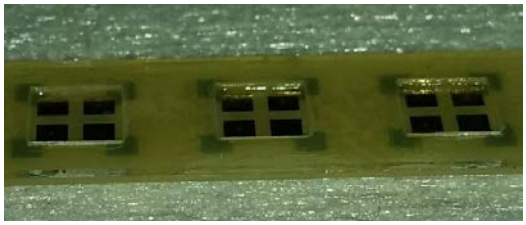

Figure 15. Cavity package test vehicle

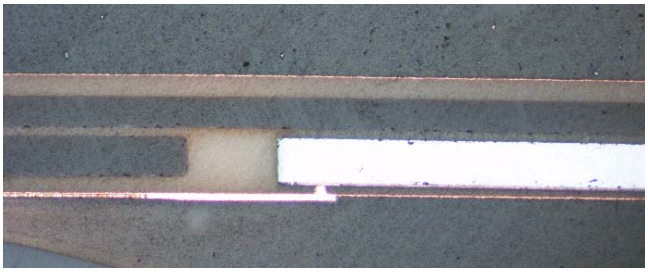

Figure 16. Cross section of the embedded sensor package test vehicle showing die embedded within ultra-thin glass cavity

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