Design and Demonstration of Power Delivery Networks With Effective Resonance Suppression in Double-Sided 3-D Glass Interposer Packages

Gokul Kumar, Srikrishna Sitaraman, Jonghyun Cho, Venky Sundaram, Joungho Kim, Member, IEEE, and Rao R. Tummala, Fellow, IEEE

Abstract—Ultrathin 3-D glass interposers with through-package vias at the same pitch as through-silicon vias (TSVs) have been proposed as a simpler and cheaper alternative to the direct 3-D stacking of logic and memory devices. Such 3-D interposers provide wide-I/O channels for high signal bandwidth (BW) between the logic device on one side of the interposer and memory stack on the other side, without the use of complex TSVs in the logic die. However, this configuration introduces power delivery design challenges due to resonance from: 1) the low-loss property of the glass substrate and 2) the parasitic inductance due to additional length from lateral power delivery path. This paper presents for the first time, the design and demonstration of power delivery networks (PDNs) in 30-µm thin, 3-D double-sided glass interposers, by suppressing the noise from mode resonances. The self-impedance of the 3-D glass interposer PDN was simulated using electromagnetic solvers, including printed-wiring-board and chip-level models. The 3-D PDN was compared with that of the 2-D glass packages having fully populated ball grid array connections. The resonance mechanism for each configuration was studied in detail, and the corresponding PDN loop inductances were evaluated. High impedance peaks in addition to the 2-D PDN were observed at high frequencies (near 7.3 GHz) in the 3-D interposer structure due to the increased inductances from lateral power delivery. This paper proposes and evaluates three important resonance suppression techniques based on: 1) 3-D interposer die configuration; 2) the selection and placement of decoupling capacitors; and 3) 3-D interposer package power and ground stack-up. Two-metal and four-metal layer test vehicles were fabricated on 30- and 100-µm thick panel-based glass substrates, respectively, to validate the modeling and analysis of the proposed approach. The PDN test structures were characterized up to 20 GHz for plane resonances and network impedances, with good model-to-hardware correlation. The results in this paper suggest that the ultrathin 3-D interposer PDN structure can be effectively designed to meet the target impedance guidelines for high-BW applications, providing a compelling alternative to 3-D-IC stacking with the TSVs.

Index Terms—3-D interposers, glass interposers, logic memory bandwidth, power delivery, through-package-vias, TSVs.

I. INTRODUCTION

THE continuous increase of data-intensive smart mobile applications demand an exponential growth in logic-to-memory bandwidth (BW) from 5 GB/s today to an estimated 50–200 GB/s in the next decade [1], [2]. However, the reducing size of devices necessitates that such a need must be achieved with: 1) low power consumption; 2) ultraminaturized form factor; and 3) low cost. Consequently, such progress is targeted to be accomplished through the 3-D stacked ICs (3-D-ICs) comprising of a logic die and a high-BW memory-stack, interconnected by through-silicon-vias (TSVs) with wide I/O channels (500–2000). This approach enables the shortest wire-length, highest I/O density, and reduced power-consumption [3], [4]. While the TSV-based 3-D ICs provide several revolutionary benefits, they face certain drawbacks such as: 1) the need for the expensive TSVs in the logic die [5], [6]; 2) thermal-management of the logic die within the stack [7]; 3) lack of testability of the logic-memory stack to estimate a known-good-die stack [8]; and 4) the need for new wafer-based TSV manufacturing infrastructure [9]. To overcome these challenges, a simpler approach called the 3-D interposer package was proposed by Georgia Tech [10] to achieve the same BW as 3-D-IC stacks without the need for TSVs in the logic die. Such a configuration, as shown in Fig. 1, allows the integration of logic and memory dies separately on either side of an ultrathin double-sided interposer, with TPVs at the same I/O density as TSVs in 3-D-ICs. There has been significant progress with the fabrication of ultrathin glass substrates to enable the high-speed formation and metallization of ultrafine-pitch TPVs [11]. Glass is an excellent insulator with a dimensionally stable, smooth low-profile surface; thus enabling very low signal loss and coupling [12], and high I/O density similar to TSVs in Si. Furthermore, glass substrates can be processed on large panels and eventually from roll-to-roll processing, resulting in an estimated lower cost by a factor of 5–10× over wafer-based back end of line (BEOL) silicon interposers [13], [14]. Moreover, unlike the conventional interposers that require an additional
PDN network and 2) parasitic inductance due to lateral power delivery paths. These factors lead to the increased magnitude and number of resonant peaks in the PDN impedance profile, potentially resulting in rapid voltage fluctuations at high current densities, and increased simultaneous switching noise (SSN). Consequently, careful PDN design is necessary to ensure high BW in 3-D glass interposers.

P/G plane resonances due to high-Q substrates and techniques to mitigate the same have been extensively studied in the past decade for organic packages [15], [16]. A preliminary investigation of these effects with glass substrates was reported in [17]. More recently, the resonances in glass interposers were analyzed and compared with silicon and organic interposers [18]. The effects of signal discontinuity on substrate resonances were analyzed through multilayer finite difference method modeling [19]. These results indicate that resonance suppression in glass interposers is more challenging than in silicon, where the relatively higher conductivity of Si (10–20 S/m) reduces the resonance magnitude due to the associated high loss. The signal and power integrity in glass interposers with a large number of signal I/Os using through–via transitions have been studied and compared with those in silicon interposers [20]. Based on this analysis, the SSN was identified as a major design challenge in glass interposers. The PDN design techniques to improve the signal return-path, including the placement of discrete decoupling capacitors and ground vias were investigated in [21]. However, further analysis specific to double-sided 3-D glass interposers is required to determine the impact of increased resonant peaks on power integrity.

Previous studies on the impact of reduced P/G BGAs on PDN design showed a corresponding increase in the PDN loop inductance [22]. Variation in BGA placement also contributed to a 5–15% increase in the overall PDN impedance [23], [24]. Hence, it becomes critical to study the increased inductive impedance attributable to the 3-D interposer structure. The design and demonstration of double-sided packages with lateral power delivery has been traditionally focused on board level design [25]. Based on this approach, organic feedthrough interposers having a 3-Gbps channel with 50 μm-pitch flip-chip connections were developed for integrating a memory stack with the logic die [26], [27]. Recent studies have focused on the PDN design of double-sided organic packages with six redistribution layer layers having a 512 wide I/O memory interface to achieve an aggregate peak BW of 256 GB/s [28]–[30]. The package IR drop and PDN inductance (12–200 pH) for eleven different power supply rails were quantified. In addition to organic 3-D interposers, silicon interposers-based 3-D SiPs have been proposed to meet the requirements for high routing density [31], [32]. PDN impedance and simultaneous switching output noise characteristics of a 3-D Si interposer with a 4-K TSV channel have been reported [33]. The antiresonance peak of overall PDN impedance was extracted at 80 MHz, and a phase-clocking scheme was implemented to reduce the switching current noise. The prospect of panel-based polysilicon with thick organic liners, as a low-loss substrate for 3-D interposers, has also been reported [34]. The authors previously per-
formed a comparative analysis of the resonance characteristics of 3-D interposers using different substrate materials [35]. Suppression techniques including the use of coaxial vias within the glass substrates were also examined [36].

This paper goes beyond previous studies to present the modeling, design, fabrication, and characterization of power delivery networks, to achieve high BW in ultrathin double-sided 3-D glass interposers. The first measured comparison of PDN impedance between 2-D and 3-D glass substrates is also presented. The impedance characteristics are investigated at chip, package, and board-levels. The placement of high-density capacitors embedded within the glass interposer is analyzed to suppress resonances at mid-frequencies from 0.1 to 1 GHz. A PDN stack-up is introduced with P/G plane pairs across each build-up in a four-metal-layer glass interposer, to achieve 10× reduction in the inductive impedance. The impact of design variations on the self-impedance profile is evaluated for variations in die placement, stack-up definition, and the placement of decoupling capacitors. In addition to the 3-D interposers, the techniques presented in this paper can also be applied to the PDN design of single chip 2-D packages and multichip glass interposers.

The rest of this paper is organized as follows. Section II investigates the PDN impedance of 3-D glass interposers by combining individual P/G planes modeled using 3-D EM solvers. The change in resonances due to the double-sided 3-D interposer structure, and with the addition of on-chip PDN is evaluated. The impact of resonance suppression techniques on the design of 3-D glass packages is reviewed in Section III. Section IV reports the fabrication and electrical characterization of 3-D interposer PDN using glass substrate test vehicles. Section V presents the summary and conclusion.

II. INVESTIGATION OF 3-D GLASS INTERPOSER POWER DELIVERY RESONANCES

The 3-D interposer package provides the PDN design advantages over organic and BEOL interposers with: 1) a unified entity for interposer and package PDN; 2) increased density of package P/G TPVs and chip-level C4 interconnections compared with organic packages; 3) the ability to integrate on-package decoupling capacitors that require higher temperature processing than possible with organic interposers; and (d) thick P/G planes (5–8 μm) compared with silicon interposers, on a thin package core (20 μm) to minimize resistive and inductive impedance. Still, the presence of P/G resonances poses a fundamental challenge in achieving a low impedance PDN, which leads to associated power and signal integrity problems. In addition, careful design of high-density I/O signals with through–via transitions is necessary to minimize the resonances due to return path discontinuity.

This section investigates the self-impedance (Z11) profile of double-sided 3-D glass interposer power delivery network (3-D PDN) and thoroughly examines the P/G resonances as the critical step toward clean power delivery. In this paper, the term 2-D PDN was used to denote a glass interposer PDN with fully populated BGA array. The 3-D PDN denoted the glass interposer PDN with centrally depopulated BGA array. The basic block diagram for a 3-D PDN is shown in Fig. 3, which consists of three parts: 1) package P/G planes with lateral traces; 2) TPVs; and 3) decoupling elements. P/G planes form the basis of the glass-interposer PDN, since the inductances of the large number of parallel P/G TPVs have negligible parasitics. The magnitude of total self-impedance (Z11) was generated by interconnecting separate multiport P/G 3-D EM models with their corresponding parasitic interconnections [35]. The spatial port locations and package stack-up used for full wave simulation of the multiport glass interposer P/G planes is presented in Fig. 4. The interposer size of 17 × 17 mm² was chosen to study the 3-D PDN self-impedance and the resonance modes. The P/G planes were located in the inner two-layers.
TABLE I
PROPERTIES OF INTERPOSER PACKAGE MATERIALS
FOR SIMULATION AND FABRICATION

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric Constant ($e_r$)</th>
<th>Loss tangent ($\tan \delta$)</th>
<th>Thickness (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Borosilicate Glass</td>
<td>5.5</td>
<td>0.006</td>
<td>30 μm; 100 μm</td>
</tr>
<tr>
<td>ZEONIT™ ZS polymer</td>
<td>3.1</td>
<td>0.005</td>
<td>3 μm; 8 μm; 17.5 μm</td>
</tr>
</tbody>
</table>

Fig. 5. Self-impedance for on-chip grid, glass interposer package, and PWB P/G planes from [35].

across the core to provide mechanical stability. Copper planes having a thickness of 10 μm were used in this paper. The study of PDN resistance to dc was not focused on, due to the small value of the plane resistance ($IR$-drop) similar to organic packages. The electrical properties of materials used in the simulation and fabrication of the glass interposer packages are tabulated in Table I.

The simulated self-impedance observed at the center of on-chip grid, glass interposer, and PWB P/G planes are presented in Fig. 5. It can be seen that 30-μm glass interposer with P/G planes had the lowest impedance. The effective permittivity of the P/G plane cavity was computed based on the method presented in [18]. Since the microwave modes are determined by the properties of the P/G cavity, it is possible to select polymer materials having the required thickness and electrical properties to achieve the desired resonance frequencies. In this simulation, the TM$_{21}$ mode was observed at the center. The glass interposer P/G plane capacitance and the plane inductance were extracted from the value of the first series resonant frequency.

This study was extended to evaluate the self-impedance of a 2-D and 3-D PDN without the effect of on-chip P/G grid and PWB. The schematic of the simulation and the results are shown in Fig. 6. The PDN simulations for different PDN configurations were performed in Agilent ADS after combing the multiport 3-D-EM models with lumped parasitic values. Parasitic inductances were added to the port locations based on the total number of parallel BGA connections for each configuration represented by M (700 pairs) and N (300 pairs). The multiport glass package model was then grounded at port locations based on BGA configuration. For instance, the 3-D-PDN configuration was attached to the board level represented by ideal ground with reduced number of P/G BGAs (N due to the placement of the die as shown in the schematic from Fig. 6. The interaction between the P/G plane cavity and the lateral trace generated much larger antiresonant peaks: 180 Ω for 3-D PDN versus 5.6 Ω for 2-D PDN. Additional loop inductance was also observed due to the reduction in the total number of BGAs. In addition, the first antiresonant frequency in the 3-D PDN was shifted to a lower frequency (6.2 GHz). This caused the overall core-PDN BW to be reduced by 2 GHz at the interposer due to the proposed double-sided approach. Hence, meticulous suppression of PDN resonances and appropriate signal routing is necessary to suppress SSN. However, the parasitic inductance of the lateral trace was smaller than the P/G planar capacitance, leading to high-impedance peaks only at frequencies beyond 6 GHz. The differences between higher order modes were negligible at very high frequencies beyond 15 GHz.

The self-impedance ($Z_{11}$) of the overall system as seen from center of the on-chip P/G grid was simulated by combining multiport 3-D EM models of hierarchical PDN elements from Fig. 5. The analysis was performed from die model through C4, package P/G planes, BGAs, and terminating at the board P/G planes. The simulation schematic used to perform the overall-PDN analysis are shown in Fig. 7. The PDN configurations of 2-D and 3-D interposers were estimated
based on variation in the number of package-PWB port connections. The system PDN was observed to be the sum of its individual P/G elements. Resonances were observed for the 3-D-PDN configuration near 7.3 GHz, as shown in Fig. 8, which created high impedance antiresonant peaks. The impedance comparison before and after the addition of on-chip (die) PDN is shown in Fig. 9. The resonant peaks in the interposer + PWB PDN were directly correlated with the high-impedance peaks observed in the overall-PDN as shown in Fig. 9. However, the magnitude of the self-impedance observed at the on-chip location (die + interposer + PWB) was reduced by 4 \Omega when compared with the interposer + PWB PDN. This effect was attributed to the high value of on-chip impedance at frequencies beyond 4 GHz, which dominated the overall-PDN profile. Since the transient current demand from the on-chip core-PDN at such frequencies is negligible, this result suggests that the impact of BGA reduction on overall core-PDN system impedance is minimal. However, suppression methods are still necessary at all frequencies in order to meet the target impedance guidelines.

### III. Proposed Resonance Suppression Techniques

In this section, three effective design techniques to suppress power plane resonances across a wide frequency range are proposed and verified. The first method analyzes the PDN impedance profile based on variations in the interposer BGA arrangement due to die placement. The second method examines the selection and placement of discrete and embedded decoupling capacitors within the glass substrates. The final method introduces a new package stack-up for 3-D interposers having four power delivery layers with two plane pairs across the thin-film build-up to achieve 10× reduced inductive impedance.

#### A. 3-D Interposer Die Configuration

The impact of self-impedance from two alternate BGA arrangements based on die-placement was compared, as shown in Fig. 10, without the on-chip P/G grid and the PWB. The port assignment locations and number of P/G BGA pairs for each configuration are also detailed. The first variation (type c in Fig. 10) was designed to have the same number of P/G BGAs as a 2-D interposer with full BGA array (type a in Fig. 10). Such a configuration can be achieved by employing finer-pitch BGAs or an increased interposer size. By increasing the BGA pitch in the 3-D PDN, the impact of lateral PDN path on the PDN profile can be studied, without changing the number of BGAs. The second variation (type d from Fig. 10)
was designed to allow access to center of the interposer by splitting the bottom die into two smaller dies while having a reduced number of BGAs compared with the 2-D interposer. This split die approach to 3-D PDN facilitates to study the impact of changing the number of P/G BGAs.

The high-impedance antiresonant peak observed in 3-D PDN was suppressed effectively using the proposed approaches. The magnitude of resonance suppression using split die configuration (type d) was much larger than using the finer-pitch 3-D PDN (type c) approach. Thus, the lateral trace inductance had a much larger impact on the self-impedance profile compared with the inductance of parallel BGAs. Hence, the use of multiple smaller dies to facilitate placement of P/G BGAs at the center of the interposer, minimizes the IO-PDN resonances at the package level; than using a single large die. This technique is effective in reducing the antiresonant peaks above 5 GHz. However, inductive impedance below 5 GHz cannot be suppressed by this method due to the inherent package parasitics.

B. Selection and Placement of Discrete and Embedded Decoupling Capacitors

The selection and placement of decoupling capacitors to reduce the PDN inductive impedance is a critical element in PDN design. This section evaluates the effect of decoupling capacitors on the PDN impedance of 3-D glass interposers. Three locations for on-package decoupling capacitors are shown in Fig. 11. The land-side placement of discrete capacitors at the underside of the package is restricted due to the presence of the die and the BGAs. Surface mount technology (SMT)-based discrete capacitors in 3-D interposers are ineffective at higher frequencies greater than 0.1 GHz due to their longer power delivery path and high equivalent series inductance (ESL), as shown in Fig. 11. Therefore, the embedded decoupling capacitors using component or thin-film technologies [37], [38] are most suitable to provide effective high-frequency decoupling.

The ESL-limitations of discrete decoupling capacitors at higher frequencies in glass interposers is shown in Fig. 12. Discrete capacitors with lower-ESL (example: 0402 and 0201) could be used to suppress the higher frequency resonances. However, the loop-inductance due to placement restrictions from double-side die attachment still restricts the effectiveness of low-ESL discrete decoupling capacitors at higher frequencies beyond 1 GHz. Different capacitor values of 1 nF, 82 pF, and 1.2 pF were chosen to study the decoupling impact at multiple frequencies. The capacitors were mounted on SMT-compatible copper pads located at two locations—2.5-mm inward from the edge of two nonadjacent sides of the interposer. Capacitors having a value of 1 nF was found to be effective in reducing PDN impedance up to 0.1 GHz. However, the effect of 1.2-pF SMT capacitor was not observed on the PDN measurement, due to its small value and high resonance frequency, which was superseded by the test structure inductance. To address these placement challenges, the integration of embedded capacitive materials has been explored in glass substrates. These materials can be processed at higher temperatures due to the inorganic nature of glass, similar to silicon interposers. The uniform placement of 1 nF embedded and SMT-type decoupling capacitors across a glass package is examined in Fig. 13. While both the embedded and SMT-type capacitors provided resonance suppression at frequencies below 0.1 GHz, embedded capacitors were observed to provide lower inductive impedance up to 1 GHz. Hence, the embedded capacitors can be employed as a miniaturized and more effective alternative to discrete SMT-type capacitors for 3-D interposer decoupling applications [37].

C. 3-D Interposer Package P/G Stack-Up

The optimization of P/G planes in a glass interposer stack-up was studied to improve power integrity. This approach has been widely researched [39], since it provides distributed capacitance very close to the die, with low ESL and without additional space requirements. In addition, the multiple power or ground layers in ultrathin glass interposers can be interconnected using multiple parallel TPVs and blind vias having very low effective inductances. A schematic view of the substrate cross section and the location of TPVs employed in this paper are shown in Fig. 14. The P/G plane.
Fig. 13. Comparison between embedded and SMT-type decoupling capacitors.

Fig. 14. PDN setup for four metal layer P/G.

Fig. 15. Self-impedance comparison of four metal layer PDN.

Fig. 16. Self-impedance comparison of 3-D PDN of package stack-up with ideal PWB.

This study was extended as shown in Fig. 16, to compare the self-impedance profile of complete system PDN, for two-metal and four-metal P/G stack-up of 3-D PDN by assuming ideal PWB and Voltage regulator module (VRM) behavior. The proposed four-metal P/G planes were proved to reduce the magnitude of the high-impedance peak in 3-D interposers from 180 to 0.9/Ω, providing effective mitigation of P/G resonances in 3-D interposers. While the overall impedance magnitude of four-metal P/G planes was 10× lower at all frequencies under consideration, an additional parallel resonance was observed at lower frequencies (few GHz) due to the interaction of the lateral inductance of the planes with the capacitance between the build-up metal layers (M1–M2). This effect was further examined in Fig. 17, which compares the impedance profiles of four-metal layer 2-D and 3-D PDN. These resonances can be minimized by optimizing the placement of the P/G TPVs that are used to interconnect the planes. The use of thinner build-up layers (1–5 μm) was also shown to provide complete suppression of P/G resonances across a wide-frequency range.

A comparison between the different PDN resonance suppression techniques that were investigated in this paper is
TABLE II

<table>
<thead>
<tr>
<th>Interposer Configuration</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type B) 3-D PDN</td>
<td>N/A</td>
<td>High impedance (180 ohm) peaks at high frequencies and low PDN bandwidth at interposer level</td>
</tr>
<tr>
<td>(Type C) 3-D PDN with increased BGA Pitch (same number of BGAs as 2-D PDN)</td>
<td>2X lower magnitude of high-impedance peaks</td>
<td>More expensive package due to finer BGA and PWB compatibility</td>
</tr>
<tr>
<td>(Type D) Split Die 3-D PDN (same number of BGAs as 3-D PDN)</td>
<td>Elimination of high-impedance peaks at high frequencies</td>
<td>Die level changes needed</td>
</tr>
<tr>
<td>SMT-based Decoupling</td>
<td>Low cost</td>
<td>Large ESL, No land-side placement on double-side interposers</td>
</tr>
<tr>
<td>Embedded Decoupling capacitors</td>
<td>Can be placed under the die for optimal resonance suppression</td>
<td>Higher cost than SMT-based decoupling capacitors</td>
</tr>
<tr>
<td>Four-metal thin film P/G</td>
<td>10X impedance reduction across wide frequency band</td>
<td>Increased package layer count</td>
</tr>
</tbody>
</table>

Fig. 17. Self-impedance comparison of 3-D PDN build-up thickness variation.

Fig. 18. Comparison of 3-D interposer resonance suppression techniques.

shown in Fig. 18. It can be seen that using various design methods, PDN resonances in 3-D interposer can be completely suppressed, and thereby improving the PDN BW. The different methods are summarized in Table II.

IV. TEST VEHICLE FABRICATION AND CHARACTERIZATION

Test vehicles were fabricated on a 150 mm × 150 mm glass substrate, using panel-based double-side processes [11] to study the PDN impedance profile of the proposed glass-based 3-D interposer. The glass core was laminated with a 17.5-μm-thick ZIF polymer. The polymer layer acts a stress buffer layer and also improves the handling [11]. Electrolytic plating was used to achieve a copper thickness of 8–10 μm. Following the fabrication of the substrate, measurements were performed using a vector network analyzer with 250-μm-pitch probes, after short-open-load-through calibration. A two-port self-impedance measurement technique was used to achieve milliohm-scale accuracy [40].

A. Measurement of Power-Ground Plane Self-Impedance

To characterize the self-impedance of P/G planes in the glass interposer, two stack-up configurations were employed: 1) a glass core of thickness 100 μm, having four metal layers and 2) an ultrathin glass core of thickness 30 μm, having
two metal layers. The dimensions of the interposers were 17 mm × 17 mm and 10 mm × 10 mm, respectively. The schematic cross section of the stack-up for each configuration is shown in Fig. 19. The P/G planes were fabricated on either side of the polymer-laminated glass core containing TPVs. The details of the individual P/G plane coupons and port locations are shown in Fig. 20.

The sample was probed on the top metal layer (M1) as shown in Fig. 20(a) using pads connected to the planes through blind vias and TPVs. The self-impedance (Z11) measured at the center of the 17 mm × 17 mm P/G planes, across the 100-μm-thick glass is plotted in Fig. 21. The mode resonances were in agreement with the simulation results. The shift in the first series resonance of the measured impedance can be attributed to variation of the metal thickness and that of the dielectric layers during fabrication. Overall, there was good correlation between the simulated and measured responses. The magnitude of the mode-resonant peaks in the measured results was suppressed due to the contact resistance of the probe pads.

P/G planes of dimensions 10 mm × 10 mm were fabricated using ultrathin glass having a thickness of 30 μm; to demonstrate the effects of change in interposer stack-up, on the PDN self-impedance. The self-impedance and transfer impedance (Z21) measured at ports located near the edge of the P/G planes, are shown in in Fig. 20(b). This was used to study the overall plane impedance. These results are shown in Fig. 22. There was excellent correlation between the measured and simulated responses for both plots. The capacitance and inductance of the PDN were lower owing to the smaller size of the planes, leading to a shift of the mode-resonances to higher frequencies. The improved suppression in this case occurs due to the thickness reduction between the P/G layers, when compared with the previous 100-μm-thick glass.

The effect of P/G plane size variation in glass substrates was studied in Fig. 23. The measured self-impedance of three different substrate sizes were compared with the ports located near 0.5 mm inside the central edge. A smaller interposer size (7.5 mm × 7.5 mm) was added to this comparison based on the 30-μm-thick glass stack-up. The smaller size (7.5 mm × 7.5 mm) of the interposer resonates at a much higher frequency compared with larger interposers, due to the change in resonance cavity dimensions. This technique is different from the layer thickness cavity dimensions. However, there is also a reduction in the total plane capacitance with smaller size P/G planes, similar to the observation in the previous example.
Fig. 23. Comparison of measured self-impedance ($Z_{11}$) for P/G planes of multiple sizes across 100 and 30-$\mu$m glass.

Fig. 24. Cross section of SMT decoupling capacitor placement on P/G planes in 100-$\mu$m glass interposer.

Fig. 25. Decoupling capacitor placement on P/G planes (a) top view and (b) probe arrangement.

B. Resonance Suppression With Discrete Decoupling Capacitors

To verify the impact of decoupling capacitors on resonance suppression, four SMT-type decoupling capacitors ($2 \times 1$ nF and $2 \times 1.2$ pF) were mounted on the top layer of the 100-$\mu$m-thick sample. Two capacitors were mounted on each pad to reduce the ESR, and were connected to P/G planes using TPVs. The cross section of the decoupling capacitor after mounting is shown in Fig. 24. The measurement was performed at the center of the plane, with the capacitor SMT pads located 2.5 mm away from the edge of the planes, as shown in Fig. 25. This location was chosen in order to represent a 3-D-PDN configuration with a bottom mounted die, which restricts the placement of the land side capacitors near the center of the interposer. The self-impedance with and without decoupling capacitors is compared in Fig. 26. The capacitors affected decoupling at frequencies below 1 GHz. However, at 1.4 GHz, a new high-impedance peak was created due to parallel resonance between the package P/G plane capacitance and the combined ESL of the capacitors, mounting pads, blind vias, and TPVs. The 1.2-pF capacitors did not suppress high frequency resonances due to the ESL and the large trace length between the point of mounting and the center probe. Thus, SMT-type decoupling capacitors were not effective in reducing the inductive impedance at gigahertz frequencies, where additional high-impedance peaks are generated in 3-D interposers. This indicates that the placement of decoupling capacitors must be carefully designed for 3-D glass interposers.

C. Characterization of 2-D- and 3-D-PDN Impedance

Test coupons having BGA pads on the M4 metal layer were designed on 100-$\mu$m-thick glass substrates, to compare the self-impedance of 2-D and 3-D glass package PDN. In both cases, the 17 mm $\times$ 17 mm planes were modified to have an array of BGA pads at a pitch of 500 $\mu$m. The top view of the 2-D- and 3-D-PDN P/G plane coupons and BGA locations are shown in Fig. 27. The 2-D interposer was designed with a BGA array having a total of 730 P/G BGAs. Of these, 170 P/G BGAs located at the center of the interposer provided a direct PDN path to the PWB. These P/G BGA pads located within the 10 mm $\times$ 10 mm area were removed to represent the 3-D interposer PDN schematic, resulting in 560 P/G BGA connections.
In order to simulate the effects of an ideal VRM and PWB and extract the effective impedance as seen from on-chip PDN, all the BGA pads were shorted using sputtered copper having thickness of 1–3 μm. The characterization for both PDN scenarios is shown Fig. 28. The 3-D interposer PDN exhibited an overall increase in inductive impedance when compared with the 2-D scenario due to the lateral inductive path. In addition, a new high-impedance peak occurred at 7.4 GHz, which directly correlates the 3-D-PDN simulation results. This impedance peak was not prominent in 2-D-PDN configuration due to reduced inductance arising from the presence of central P/G interconnections exactly under the center (on-chip) probing location on the other side of the substrate. The high-impedance peak in 3-D PDN was not observed at frequencies below 7 GHz due to the small value of the lateral trace inductance. Hence, the 3-D-PDN structure can meet the target impedance profile for core-PDN design without significant impact, due to negligible current requirement at gigahertz frequencies.

V. CONCLUSION

This paper studied the design and demonstration of PDN resonances and effective suppression techniques in ultrathin and double-sided 3-D glass BGA interposer packages for high-BW applications. A 17 mm × 17 mm 3-D interposer PDN was modeled using multiport full-wave 3-D EM simulations. Additional resonances were observed near 7.3 GHz, due to the interaction of the increased lateral inductance with the resonant cavity. These high-impedance peaks in the PDN profile of 3-D interposer systems were observed to be mitigated due to the domination of the on-chip capacitance at gigahertz frequencies. Nevertheless, suppression methods were necessary to meet the target-impedance guidelines and reduce SSN. Three primary design techniques to address this problem were proposed and studied. Placing low-ESL decoupling capacitors was effective in reducing impedance within the 0.1–1 GHz range. Providing central P/G connections using more than one die at the underside of the glass interposer was most effective to suppress the high-impedance resonance peaks beyond 5 GHz. In addition, the magnitude of the inductive impedance was reduced by over 10–4 due to a through-package-vias at same pitch 3-D glass substrates with TPVs to enable a simpler approach for achieving high I/O high BW compared with 3-D-ICs with TSVs.

REFERENCES


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