

Innovative Electrical Thermal Co-design of Ultra-high Q TPV-based 3D Inductors in Glass Packages

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Abstract—This paper introduces an innovative concept of electrical-thermal co-design for high-Q 3D inductors using through-package-via (TPV)-based copper networks in ultra-thin power amplifier-integrated glass modules. The copper networks are designed to provide high quality factor inductors, and also simultaneously enable heat transfer in ultra-miniaturized glass packages. Such TPV-based 3D inductors achieved the highest Q factor (>150 @ 1 GHz, >200 @ 2.4 GHz, SRF > 25 GHz), 7 times greater than that of the state-of-the-art package embedded inductors at LTE frequencies. The thermal structure, with power amplifier die assembled onto it, also reduces the package size by placing the embedded TPV-based inductor adjacent to it without affecting its Q.

Keywords: 3D Inductor; Through-package-via; Heat-transfer; Glass Packages

I. INTRODUCTION

Integrated multi-mode multi-band (MMMB) subsystems face three fundamental challenges for miniaturization and performance improvement – inadequate quality (Q) factor of thin-film components, electromagnetic interference (EMI) issues and difficulties in heat dissipation. Q factor degradation comes from several factors such as substrate losses, increasing the ratio of resistance to inductive reactance because of skin effect, proximity and parasitic capacitance between tightly-spaced conductors. Thus, it is inevitable to place the inductor off the chip, and in the package, to overcome the constraints from limited on-chip real-estate and high losses. Moreover, it is beneficial for the components to utilize the substrate volume in all three (X-Y and Z) directions. Therefore, size-performance trade-off in the components can be enhanced with more flexibility in the design options [1].

State-of-the-art on-chip inductors [2][3] utilize single or multilayered spiral structures on-chip, with low Q factor. Package-integrated inductors [4][5] achieve high Q but utilize thick metal and dielectric structures leading to low component densities. This paper demonstrates TPV-based 3D inductors, with innovative thermal structures to cool the power amplifier die with the minimum packaging size. Such a co-design can result in high Q inductor, and also minimizes the need for bulky active and passive cooling technologies, which include heat-sinks, micro-fluidic channel cooling and PCM cooling [6][7][8].

This paper, thus, demonstrates an innovative concept of electrical-thermal co-design for embedded ultra-high Q factor inductors, along with efficient thermal structures in glass packages. Since the concept involves a combination of two structures, the paper introduces each electrical and thermal component separately, and compares the performance when they are optimally placed together.

II. 3D INDUCTORS

Traditional spiral inductors can achieve high inductance density by winding copper traces as 2D coplanar or 3D multilayer coil structures, while achieving relatively good Q factor (~ 40) by designing with the proper ratio of line width and spacing. Despite the ease in controlling the inductance density and achieving adequate Q factors for certain RF applications, 2D inductors still face trade-offs in simultaneously achieving high Q and inductance density because the inductance density is severely compromised with large and thick metal structures.

In order to achieve higher Q factors, it is required to have more induced magnetic flux while keeping the resistance as low as possible. Through-Package-Vias (TPVs) with 100 μm diameter have much more surface area than conventional trace-based inductors. Thus, they can minimize the increment in resistance due to skin effect as the operating frequency increases. Moreover, they reduce the eddy current loss because the larger distance between TPVs can suppress the induction of any magnetic coupling in the adjacent copper networks. Furthermore, it can utilize unused Z directional space of the packaging rather than planar area in the same level.

In the previous TPV-based daisy-chain inductor designs [9][10], the TPVs were connected such that the signal path between two ports was long enough to have a good inductance density [Fig. 1(1)]. The path of the current starts from one port to the other, based on the way the copper pads joined together. The path is illustrated with guided arrows in Fig. 1(1).(b) and (c).

However, with the inductors introduced in this paper [Fig.1.2], all the via-capturing pads were shorted to each other on both top and bottom layers to form a net-like structure with TPV pillars. By doing so, the structure can significantly reduce the length of AC current path throughout the conductor, which in turn minimizes leaky

magnetic flux with signal traveling between the two ports. It is essential to reduce the leaky magnetic flux because it could induce eddy current among the nearby copper networks. Moreover, the reduction in DC resistance is far greater than the drop in inductance, which can result in higher Q factor since Q factor is the ratio of induced magnetic flux to the resistance at a specific frequency.

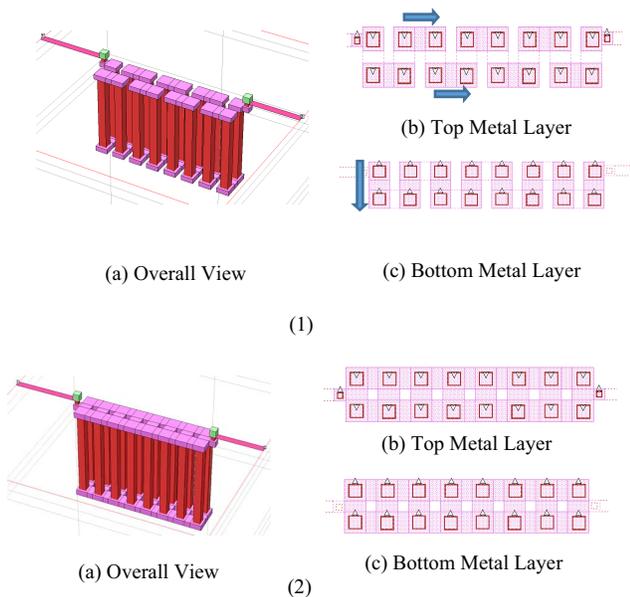


Figure. 1. 3D TPV-based Inductor: (1) prior-art, and (2) new inductor.

III. INDUCTOR SIMULATIONS AND ANALYSIS

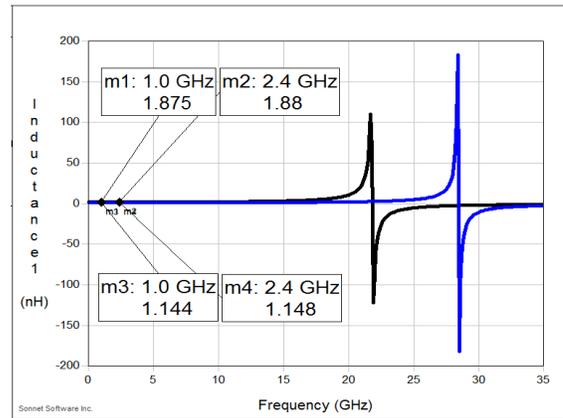
The prior art of 3D inductor and modified inductor are modeled and simulated using EM Solver-Sonnet. For both cases, there are 4 metal layers, M1-M2 on the top of the glass, and M3-M4, on the bottom of the glass. The structure was embedded into the package so that only M2 and M3 layers were used and connected through TPVs. The specs and performance of each type of inductor are shown in TABLE I.

TABLE I. INDUCTOR SPECIFICATIONS FOR 3D INDUCTORS

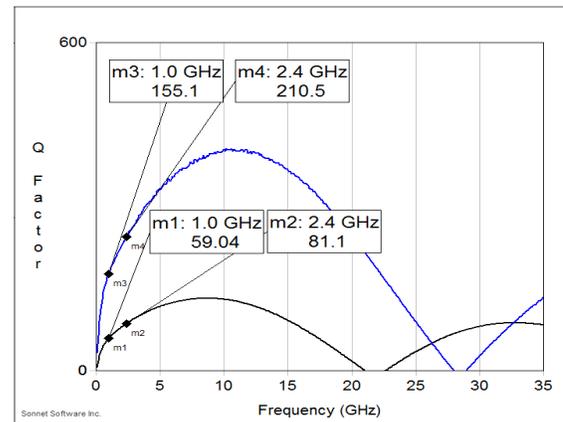
Specifications	3D Inductors	
	Prior-Art(Fig. 1) (@1GHz/ @2.4GHz)	New Inductor (Fig. 2) (@1GHz/ @2.4GHz)
Inductance	1.875nH/ 1.88nH	1.144nH/ 1.148nH
Q factor	59.04/ 81.1	155.1/210.5
SRF	21.7GHz	28.4GHz
Inductor Size	1.84mm x 0.39mm	1.84mm x 0.39mm
Height including stack-up	0.146 mm	0.146 mm
Density(Ind./ Volume)	~ 17.9nH/mm ³	~11 nH/mm ³

By shorting the copper pads on both M2 and M3 layers, the reduction in inductance is around 38% lower than the original. However, the Q factor was boosted up by a factor

of 2.6 while retaining the same height and size. On top of that, Self-Resonant-Frequency was shifted to higher values, from 21.7 GHz to 28.4 GHz so that the new inductor has wider margin before it becomes capacitive. The comparison of the simulated result for both inductors are shown in Fig.2. The blue line stands for the new inductor, and the black line shows the prior-art.



(a) Inductance Response



(b) Q Factor Response

Figure. 2. Prior-Art vs. New Inductor: (a) inductance response, and (b) Q factor response.

Thus, 3D inductors successfully improve the inductor performance by utilizing area in Z direction of the substrate. These TPV inductors can be integrated in glass as 3D Integrated Passive Devices (3D IPDs) or 3D embedded LC components in 3D Integrated Passive and Active Component (3D IPAC) modules.

IV. 3D INDUCTOR WITH THERMAL STRUCTURES

Glass is an excellent RF material, especially for its low-loss, surface smoothness and dimensional stability for precision impedance matching, but the disadvantage comes from its low thermal conductivity. Thus, it is critical to

embed highly-efficient thermal structures when glass packages are designed. An array of copper TPVs are designed to create the thermal structures. However, these thermal structures can degrade the electrical performance due to their coupling with the inductors. Therefore, in addition to the heat dissipation characteristics of the thermal structures, the electrical performance of 3D inductor was also studied when it is placed in proximity with the thermal structure.

The 3D inductors and thermal structures were spatially separated with different parallel or orthogonal placements. Such a study in components layout could provide critical information regarding how much the coupling effect can deteriorate inductance density and Q factor depending on the spatial configuration. It is imperative to have two components optimally placed such that the effect of induced magnetic flux from 3D inductors is minimum.

In Fig. 3(a), the 3D inductor is arranged such that is parallel to the thermal structure, thereby minimizing the packaging area. Fig. 3(b) shows that the inductor is placed in an orthogonal direction to the thermal structure to see if there is any major difference in the electrical performance compared to the previous case.

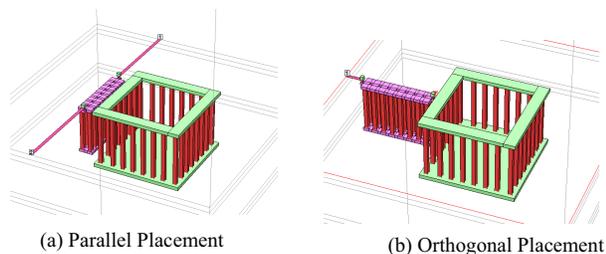


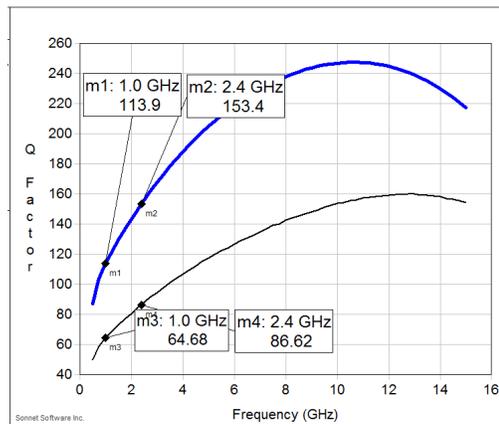
Figure 3. 3D Inductor placement with thermal structure: (a) parallel placement, and (b) orthogonal placement.

TABLE II. INDUCTOR PERFORMANCE COMPARISON

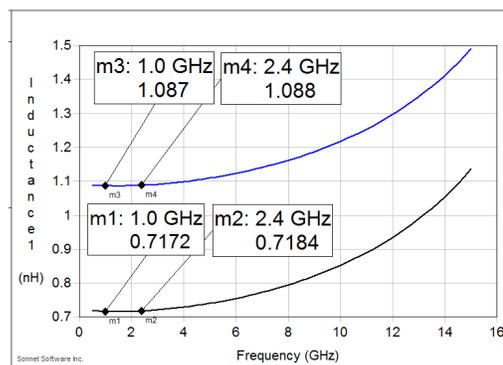
Inductor Performance Comparison			
	3D Inductor Only (@1GHz/2.4Ghz)	Parallel Placement (@1GHz/2.4Ghz)	Orthogonal Placement (@1GHz/2.4Ghz)
Thermal structure	None	Yes	Yes
Inductance	1.144nH/1.148nH	1.087nH/1.088nH	0.717nH/0.7184nH
Q Factor	155.1/210.5	113.9/ 153.4	64.68/ 86.62

The parallel placement next to thermal structure shows higher inductance density and is almost 2X better in Q factor than the orthogonal placement. For this case, the coupling effect between the inductor and thermal structure has been less affected since only one side of the inductor is adjacent to the thermal structure. On the contrary, in the orthogonal placement case, the induced magnetic flux from both sides of the inductor suffer from cross-talk with the thermal structure, and the amount of coupling effect is much greater. Therefore, the parallel placement is not only good

for its smaller packaging area, but also guarantees higher inductance density and Q factor as shown in TABLE II.



(a) Inductance Response



(b) Q Factor Response

Figure 4. Inductance and Q Factor Response for parallel (blue) and perpendicular (black) arrangements of inductor and thermal structures.

V. THERMAL STRUCTURE MODELING

A new concept of die-mountable thermal structure is co-designed with 3D embedded TPV inductors. The substrate comprises of four-metal layer (M1-M4) on glass with polymer build-up dielectrics – two layers (M1 and M2) on top and the rest (M3 and M4) on bottom. This thermal structure has a frame-like design around the embedded TPV inductor, where the die can be mounted onto it. Thermal TPVs connect the frame directly from M1 to the ground plane on the bottom layer M4. The model construction was completed with the aid of Finite Element Method simulation tool – COMSOL. The model was constructed to reflect actual dimensions for the thermal chip - 2.5 mm x 2.5 mm, and material properties. Fig. 5 shows five snapshots of the thermal structure, and also illustrates the path of the dissipated heat from hotspot in the die to heat spreader in the substrate and into the PCB.

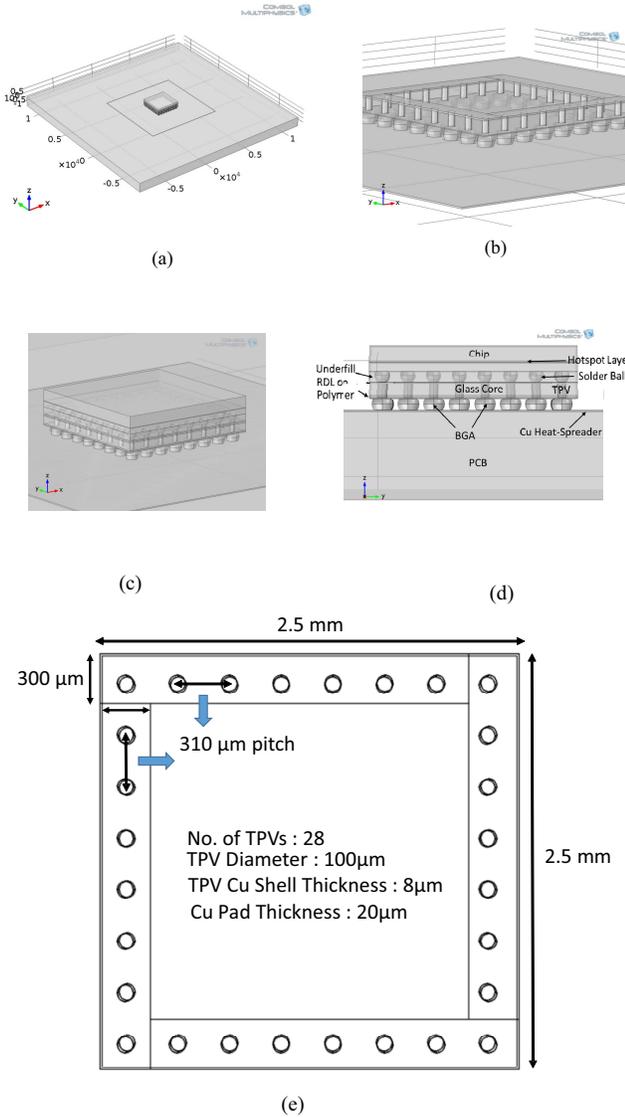


Figure 5. COMSOL model construction: (a) overall view, (b) a novel thermal structure, (c) zoomed view, (d) modeling stack-up, and (e) dimensions details of the thermal structure.

The heat is transferred throughout solder balls connecting the die to RDL on the substrate. Then thermal TPVs, which have copper shell thickness as $8 \mu\text{m}$, continue to transfer heat down to the heat-spreader on bottom side of the glass package. Lastly, BGA balls are connecting heat-spreader on package to another heat-spreader on PCB top layer. The ground copper plane simultaneously addresses two challenges, signal grounding and heat spreading. Generated heat from the hotspot in the packaged-die can be drained down to heat-spreader in the substrate and then onto the PCB layer. This innovative thermal structure accomplishes these two by transferring the generated heat from die down to the heat spreader peripherally, while functioning as a wide ground plane for the adjacent

embedded TPV inductors to this thermal structure. The materials and their properties used for the simulation are given in TABLE III.

TABLE III. MATERIALS AND PROPERTIES USED FOR THE SIMULATIONS

Materials	Properties		
	Heat Capacity [J/(kg·K)]	Density [kg/m ³]	Thermal Conductivity [W/(m·K)]
Die(Epoxy)	1000	2500	1.6
Silicon	700	2329	130
Underfill	800	1510	0.3
Solder, 60Sn-40Pb	150	9000	50
Polymer	936	2100	1
Glass	480	2200	1.1
Copper (Metal Pad, Blind Via, TPV and Heat Spreader)	385	8700	400
BGA Ball(SAC305)	2320	7370	62
FR4	1369	1900	0.3

The following boundary conditions were applied for all the simulations:

- Convection Heat Flux (Heat Transfer Coefficient): $H = 10 \text{ W/m}^2\cdot\text{K}$
- Total Power from 1W to 10W was imposed on the Hot-spot plane ($0.25 \text{ mm} \times 0.25 \text{ mm}$).
- Initial Surface Temperature = 20°C

VI. THERMAL SIMULATIONS AND ANALYSIS

In order to quantify the effectiveness of this novel thermal structure, the steady-state temperature at the hottest area was obtained by imposing various values of power stress onto the hotspot in the die. The simulation results demonstrate that the steady-state temperature on the hottest part is 35.8°C when 1 Watt of power is imposed on the hotspot (Fig. 6).

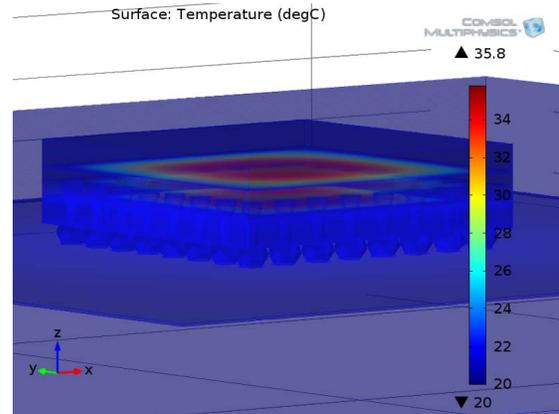


Figure 6. Thermal map of the package obtained through simulations (Power = 1W on Hotspot).

In Fig. 7, the steady-state temperature at the hottest part shows 98.8°C when 5 Watt was imposed on the hotspot as the boundary condition.

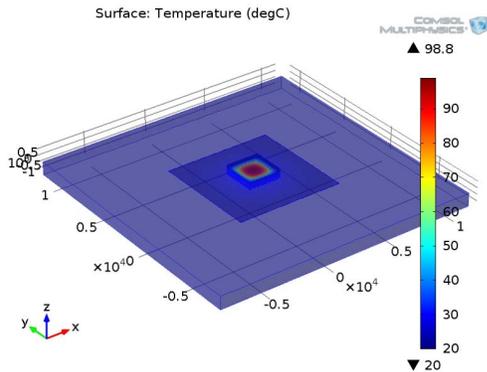


Figure 7. Thermal map of the package obtained through simulations (P = 5W on Hotspot).

The performance of the novel thermal structure was further investigated by applying various power stress conditions on hotspot plane in the die. The steady-state temperature at the hottest area in the model was plotted for each power stress condition. [Fig. 8.] As seen in the figure, the thermal structure can handle up to 4W of power while maintaining the hotspot temperatures of less than 85°C.

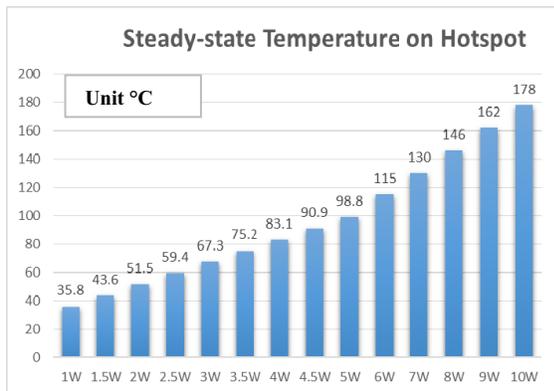


Figure 8. Steady-state temperature of hotspot with various power stress conditions.

VII. CONCLUSIONS

Innovative electrical-thermal co-design of high-Q inductors with TPVs was demonstrated for ultra-low loss matching networks in power amplifier-integrated packages. The structures incorporate thermal paths along with the TPV inductors to create efficient PA cooling. Thermal and electrical simulations were performed individually to demonstrate the benefits of the hybrid electrical-thermal structures.

Despite the coupling effects between 3D inductors and the thermal structures, the optimal TPV-based inductors could achieve Q factors of more than 100 @ 1GHz and greater than 150 @ 2.4GHz. Furthermore, the novel thermal structure could dissipate the heat from the hotspot in the die without adding size and cost constraints that are usually associated with conventional active and passive cooling devices. The steady-state temperature was as low as 35.8°C when 1Watt of power was applied on the hotspot plane. Such co-design can improve the electrical performance in RF substrates while also enhancing the reliability.

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