Signal and Power Integrity Analysis in 2.5D Integrated Circuits (ICs) with Glass, Silicon and Organic Interposer

Youngwoo Kim[1], Jonghyun Cho[1], Kiyeong Kim[1], Venky Sundaram[2], Rao Tummala[2] and Joungho Kim[1]

[1]Terahertz Interconnection and Package Laboratory, Department of Electrical Engineering, KAIST
291 Daehak-ro, Yuseong-gu, Daejeon, 305-701, Republic of Korea
youngwoo@kaist.ac.kr

[2]Packaging Research Center, Georgia Institute of Technology
813 Ferst Drive NW, Atlanta GA 30332, USA

Abstract

2.5D integration using interposer and through via technologies is one of the promising solutions to enable systems with higher electrical performance and at the same time reducing size of the whole systems. To maximize benefits of the interposer, power distribution network (PDN) and channels should be well-designed. PDN and channel properties are heavily affected by the material properties of the interposer substrate. Depending on the substrate material, anti-resonance frequency of PDN can coincide with ICs' switching frequencies. Therefore analysis and comparison of hierarchical PDN are important. Also channels can be affected by the PDN design, especially channels escaping/entering interposers are affected by the properties of the interposer PDN. Therefore, when designing interposers, co-design and co-analysis of PDNs and channels are required.

Introduction

Recently Semiconductor industries are having difficulties to overcome technical challenges associated with the performance saturation of conventional CMOS processes. For example, bandwidth of DRAM in mobile application systems or graphic modules is doubled every year due to the technical trend that requires higher bandwidth. However it is becoming a burden for industries to develop and manufacture such circuits with doubled bandwidth at the period it is needed. 2.5D integration using interposer and through via technologies is one of the promising solutions to achieve systems with higher electrical performance and at the same time reducing size of the whole systems. Interposers have finer line width and space compare to the conventional packages thus it is possible to accommodate more number of I/O channels which will increase the bandwidth of the whole system.

Especially for the application processors in mobile devices, 2.5D integration using the interposer could be a solution to routing issues which cause signal/power integrity problems since application processors accommodate tremendous amount of signal and power nets such as memory channels, HDMI and USB 3.0. For graphic modules that require much higher bandwidth compared to mobile devices, adopting interposer technologies will provide more advantages. Fig.1 illustrates cross-sectional view of 2.5D HBM module with interposer.

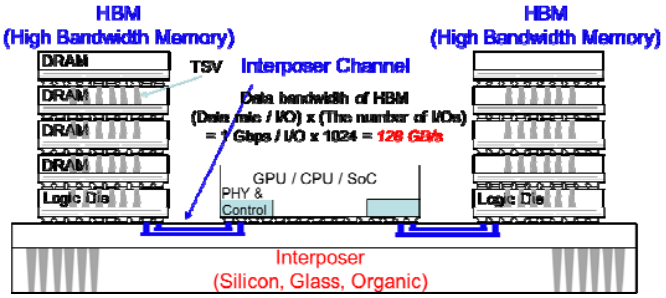


Figure 1. Cross-sectional View of 2.5D HBM module

On the interposer, each HBM is connected with SoC with 1024 interposer channels. Each channel accommodates 1Gbps bandwidth which is even lower than that of LPDDR 3, however total bandwidth dramatically increases to 128GB/s due to the total number of interposer channels. By using interposer and TSV technologies, system bandwidth can increase significantly without enhancing the performance of ICs based on CMOS technologies. When systems are formed on the interposer, its electrical performances are heavily affected by the material properties of the interposer substrate. In figure 1, possible candidates for the interposer substrate materials are also listed and advantages and disadvantages of each material is shown in the previous work [1]. When the concepts of interposer technologies were first introduced, silicon substrate was proposed since CMOS process has the longest history thus most advanced among the semiconductor fabrication processes. Therefore using silicon as an interposer substrate can enable very fine metal patterns for channels and power distribution networks [2]. However, silicon shows high insertion loss which can degrade performance of the whole system at the high frequency due to conductivity of substrate and additionally very high in cost resulting from the fine on-chip metal processes. Also the size of silicon wafer and round shape limit the yield of interposer fabrication. Another possible substrate material is organic which has been used as a semiconductor packaging material for long time. Thus low cost and low loss organic can be used as an interposer substrate. However scaling of interposer substrate thickness and width/space of signal channels are limited for the organic interposer. As an alternative of silicon and organic, glass substrate is introduce which has ultra-low loss and use panel-process which has higher yield compared to silicon interposers based on wafer processes. Even though glass

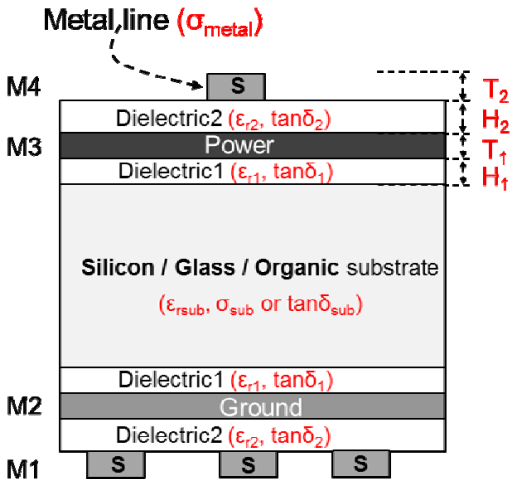
interposers are not ready for manufacturing, as technologies advance, glass substrate may maximize benefits of 2.5D and 3D Integration.

It is apparent that depending on the substrate materials of an interposer, electrical properties such as channel and power distribution network characteristics of the whole system could vary. In this paper, we first analyze and compare impedance properties of interposer PDN with glass, silicon and organic substrate. We also compare impedance properties of hierarchical PDN including 3D stacked chips, interposer and system board with different interposer substrate. In order to operate systems, providing power is crucial and operating ICs' performance is heavily affected by the hierarchical PDN impedance. Thus understanding impedance properties of hierarchical PDN is important. We also analyze signal integrity for the channels that escape through interposer since escaping signals communicate with other systems or control the system itself.

Analysis and Comparison of Power Distribution Network Impedance Properties with Different Interposer Substrate Material

In this chapter, PDN impedance properties are analyzed and compared. First, interposer PDN impedances with different substrate are compared. Also, hierarchical PDN (including 3D stacked chip PDN, interposer PDN and package PDN) impedance properties are analyzed and compared. In figure 2-(a), cross-sectional view of the interposer to be simulated and analyzed is depicted. As can be seen in the figure, 4 metal layers (M#) exist and metal layer 2 and 3 are mainly allocated for the powers and ground. Metal layer 1 and 4 are allocated for signal lines and ball/bump pads. Between power and ground planes, dielectric layers and interposer substrate exist. Material properties of metal and dielectrics are given in figure 2-(b) with physical dimensions. To simulate interposer PDN, 3D-EM solver Ansys HFSS was used. However for analyzing the hierarchical PDN impedance properties, 3D stacked chip PDN with P/G TSVs is modeled based on unit PDN models and a segmentation method. Modeling methodologies and dimensions of structures are shown with detail in the previous work [3].

Interposer with PDN size 12mm by 12mm is simulated and the impedance properties are shown in figure 3. Physical dimensions are fixed; only the dielectric1, 2 and substrate materials are changed. Under the frequency where first resonance occurs, capacitance of PDN dominated the impedance properties. Since silicon interposer has the highest value of the effective complex permittivity, PDN impedance is lower than that of glass and organic interposers. Effective permittivity can be calculated using the equation shown in [4]. In case of glass and organic interposer, effective permittivity between P/G is almost identical for the simulated dimensions, almost identical impedance properties are observed. After the first resonance, inductance of PDN dominates the impedance characteristics,



(a)

Symbol	Silicon	Glass	Organic
ε_{rsub}	11.2	5.3	4.4
ε_{r1}	3	3	4.4
ε_{r2}	3	3	4.4
tanδ_{sub}	-	0.004	0.02
tanδ_1	0.005	0.005	0.02
tanδ_2	0.005	0.005	0.02
σ_{sub}	10	-	-
σ_{metal}	5.8×10^7 s/m		
T_1	10 μm		
H_1	17.5 μm		
T_2	10 μm		
H_2	7.5 μm		

(b)

Figure 2. Cross-sectional view of interposer is shown in figure 2-(a). In figure 2-(b), material properties of metal and dielectrics are given with physical dimensions.

As frequency goes higher, mode resonances are generated.. These frequencies are determined by the size of PDN and the location of observing ports. In case of glass and organic interposer, due to low conductivity of the substrate, sharp impedance peaks are generated. Since glass substrate has the lowest conductivity, sharpest impedance peaks are generated. On the other hand, for the silicon case, due to lossy substrate, impedance peaks are not observed or relatively smaller in value compared to the other cases.

When operating chips are mounted, not only PDN impedance of chip itself affects the performance of ICs, PDN of interposer also affects the performance. Thus it is important to analyze PDN properties of the whole system.

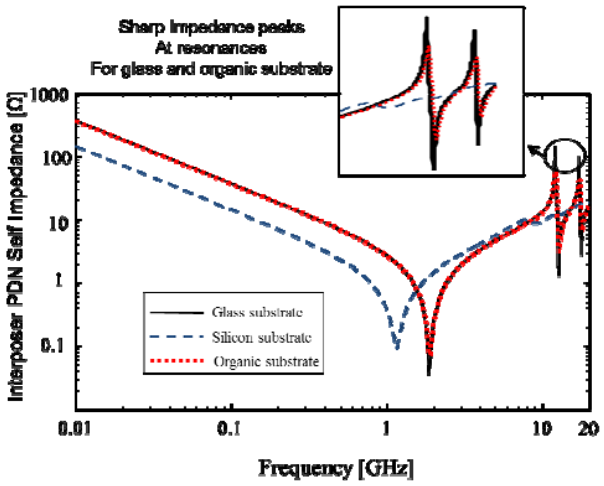


Figure 3. PDN Self-impedance seen at the center of glass, silicon and organic interposers are shown. Interposer PDN size is 12 mm by 12mm for all cases.

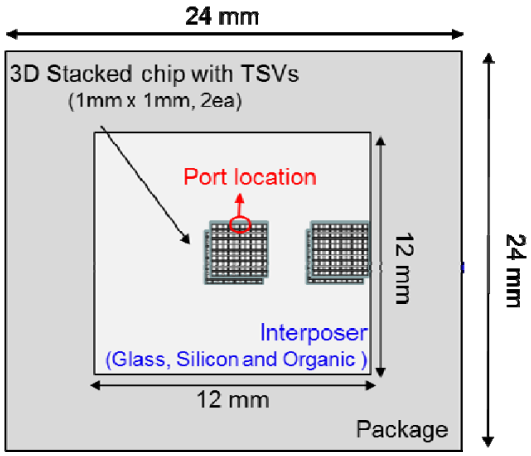


Figure 4. Top view and lateral dimensions of 2.5D IC to simulate and analyze hierarchical PDN impedance is shown.

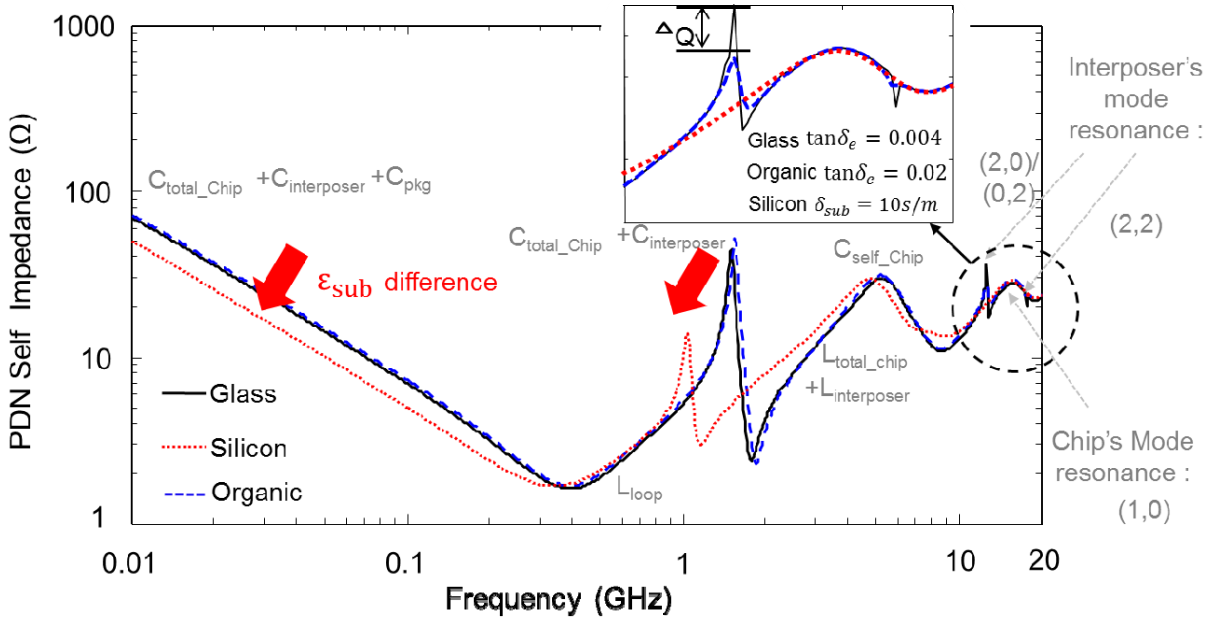


Figure 5. Impedance properties are simulated for the structure shown in figure 4. Depending on the interposer substrate material, hierarchical PDN impedance show different impedance profile.

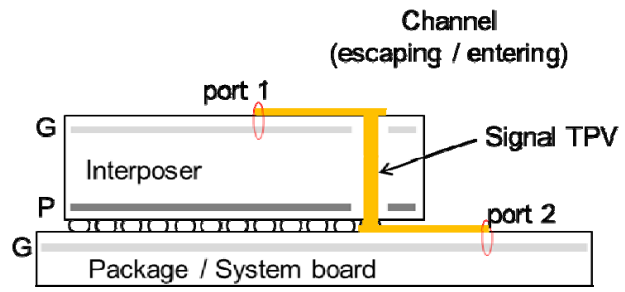
In figure 4, top view and lateral dimension of 2,5D IC to analyze hierarchical PDN impedance is shown. On the interposers, 3D stacked chips with P/G TSVs are mounted. Impedance properties are observed at the edge side of the top chip located at the center of the interposer. In figure 5, impedance properties are analyzed and the effects of interposer substrate on hierarchical PDN impedance are compared. On the graph, factors that dominate the impedance properties are listed. Since real value of permittivity for organic and dielectric mixture in glass substrate is similar, PDN impedance is almost identical for 2.5D IC with glass interposer and 2.5D IC with organic interposer. However, at the frequencies where mode resonances of the interposer appear, cases with glass interposer have sharper impedance peaks and it is due to the Q factor difference between the glass substrate and organic substrate. If silicon is used as an interposer substrate, PDN impedance is lower than other cases and it is marked with arrows in the figure 5. Also for the silicon interposer case, interposer's mode resonance aren't shown in the hierarchical PDN impedance properties due to relatively large substrate conductivity compared to that of glass and organic substrate.

We should note that on the graph, first anti-resonance occurred around 1~2 GHz. In case of the glass and organic interposer, frequency of anti-resonance is near 1.6GHz, similar to the operating frequency of LPDDR4. When designing hierarchical PDN, target impedance should be defined and proper decoupling capacitors should be placed to keep the hierarchical PDN impedance below the target impedance. Near the operating frequency of the ICs, target impedance is the lowest [5-6], which means, if the hierarchical PDN impedance violates the target impedance near these frequencies, large simultaneous switching noise (SSN) will be generated, leading to degradation of whole system's performance. This anti-resonance can be changed if the dimensions and shapes are changed, however usually in this frequency ranges, anti-resonance is generated between the loop inductance and capacitance of interposer and chip PDN. Therefore placing on-chip decoupling capacitors and interposer decoupling capacitors are crucial.

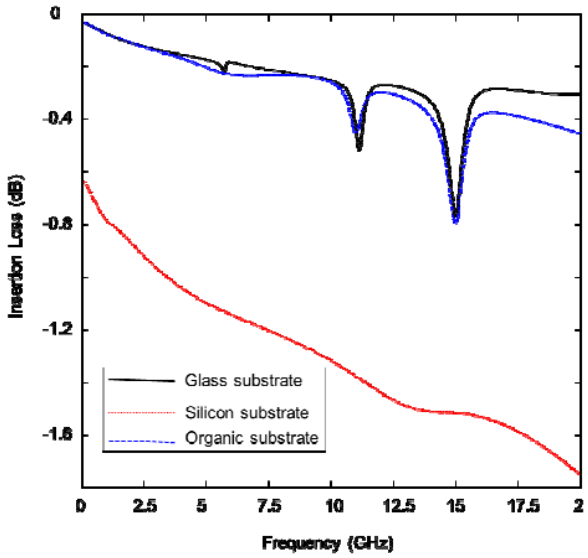
Insertion Loss Comparison of Channels Entering/ Escaping Interposers and Insertion Loss Improvement by Modifying PDN

In 2.5D ICs with interposer, many channels exist. It is possible to classify these channels into two categories: channels on the interposer and channels that are escaping (entering) of interposer. For the former case, effects of interposer substrate material on channel properties are compared in the previous work with different types of transmission line structures [7]. However, channels those are escaping (entering) are equally important since they allow system to communicate with other systems or can be used to control the systems. In this chapter, insertion loss of channel entering/escaping the interposer with different substrate is compared.

When channels escape the interposer, it should go through the TPV. When signal flows through this via, return current flows through the substrate (parasitic capacitance). Thus, when PDN resonances occur, signal quality is heavily affected by the substrate material properties. Glass interposer channel is superior compared to that of silicon and organic throughout frequencies [7] however at resonance frequencies, it becomes worse and it is well summarized in the previous work by comparing insertion loss, eye-diagram and P/G noise coupling [2,8]. In figure 6-(a), Channel escaping interposer is depicted. The diameter/height of TPV is 100um/170um and the trace of signal length on top and bottom of interposer is 1mm. Interposer PDN size is 6mm by 12mm and ground vias are placed 300um away from the signal via. In figure 6-(b), insertion loss of channels with different interposer substrate material is compared. As can be seen in the graph, Glass and organic show similar loss profile on the other hand, silicon show highest loss due to finite conductivity of substrate. At resonances, insertion loss increase for the glass and organic but it is still less than silicon. However, if the interposer size becomes larger, more loss peaks will be generated and they will shift down toward lower frequencies. Also for rouability (TPV pad is much larger than signal line's width and space), signals escaping out of the interposer are placed at the side.



(a)



(b)

Figure 6. Channel escaping interposer is depicted in 6-(a). In figure 6-(b), insertion loss of channels with different interposer substrate material is compared.

Therefore, these signals are more vulnerable to mode resonances since at the side and edge of the interposer PDN, number of modes that are allowed exist more compare to that of center. By placing more reference vias or decoupling capacitors can be solution however if these components are located, this means that space for signals decrease which will reduce the number of signal escaping. To resolve these issues, power size is modified. In power integrity point of view, designing PDN with P/G lines is not desired since it will decrease the capacitance of PDN and increase inductance and resistance of the PDN thus total revision is not desired. Figure 7 shows modified power plane to control the size of the PDN cavity. In figure 8-(a),(b) and (c), insertion loss with and without modifying the PDN for each interposer are compared. For all cases, insertion loss decrease at most frequencies. Also for the glass and organic interposer, some insertion loss peaks are suppressed totally.

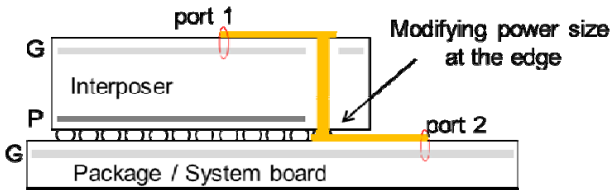


Figure 7. Modification of power plane to control interposer PDN cavity size

Conclusions

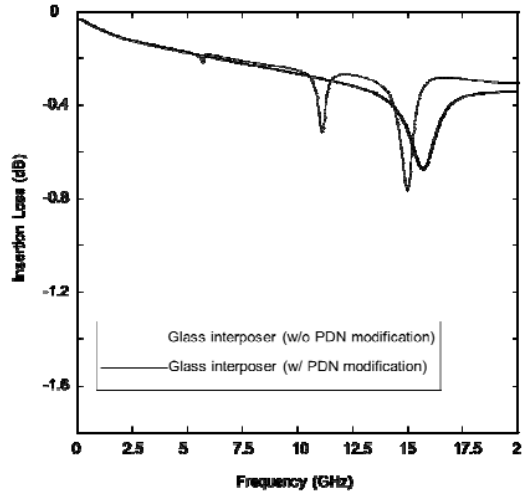
2.5D-Integration based on interposer and through via technologies is promising solution to achieve high system performance and at the same time reducing the size of a whole system. To fully achieve these advantages, PDN and channels should be well designed and these components are affected by the material properties of the interposer substrate. When designing PDN, first, hierarchical PDN impedance properties should be well estimated and analyzed to check whether impedance peaks do not coincide with switching ICs's spectrum. After the comparison, proper decoupling capacitors should be placed. Also for the signal channel design, not only channels on the interposer but also channels that enter/escape interposer should be well designed. In fact, channels that enter/escape go through the TPV should be carefully designed since it is affected by the PDN design. Therefore, when designing interposers, co-design and co-analysis of PDNs and channels are required.

Acknowledgments

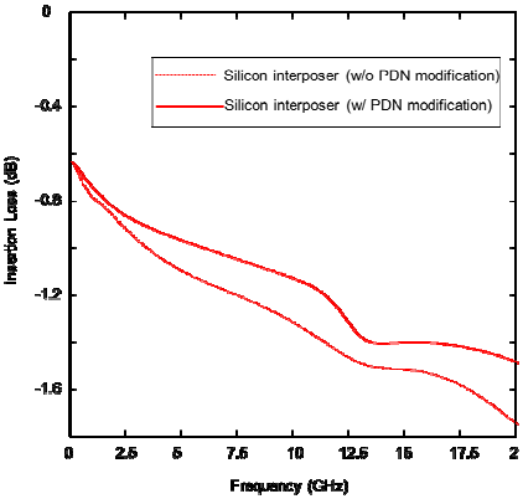
Place acknowledgments here, if needed. This work was supported by International Collaborative R&D Program (funded by the Ministry of Trade, Industry and Energy (MKE, Korea) [N0000899, Glass interposer based RF FEM for Next Generation Mobile Smart Phone] also we would like to acknowledge the financial support from the R&D Convergence Program of MSIP (Ministry of Science, ICT and Future Planning) and ISTK (Korea Research Council for Industrial Science and Technology) of Republic of Korea (Grant B551179-12-04-00). We also like to acknowledge the technical support from ANSYS for providing 3D-EM simulator HFSS.

References

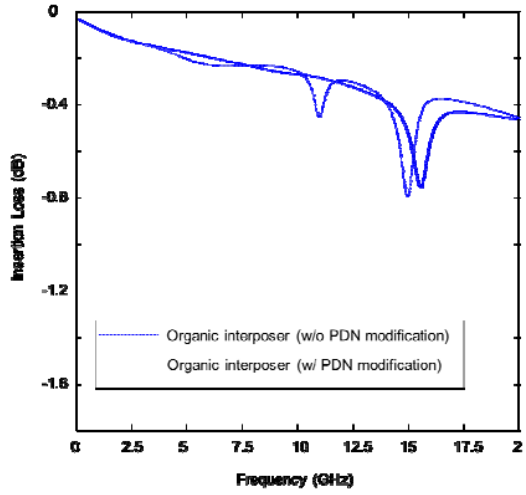
1. V.Sukumaran, T. Bandyopadhyay, V. Sundaram, R. Tummala, "Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs", *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol.2, no.9, pp.1426,1433, Sept. 2012.
2. Y.W. Kim, K.Y. Kim, J.H. Cho, V. Sundaram, R. Tummala and J.H. Kim, "Analysis of Power Distribution Network in Glass, Silicon Interposer and PCB", 2014 *IEEE International Symposium on electromagnetic Compatibility,* August. 2014, Rayleigh, NC, USA



(a)



(b)



(c)

Figure 8. Insertion loss with and without modifying the PDN for each interposer are compared.

3. K.Y. Kim, C.S. Hwang, K.K. Koo, J.H. Cho, H.G. Kim, J.H. Lee, H.D. Lee, K.W.Park, J.S. Pak and J.H. Kim, "Modeling and Analysis of a Power Distribution Network in TSV-Based 3-D Memory IC Icluding P/G TSVs, On-chip Decoupling Capacitors, and Silicon Substrate Effects", *IEEE Trans. On Components, Packaging and Manufacturing Technology*, vol.2, No.12, pp.2057-2070, December 2012
4. E. Tuncer, Y.V. Serdyuk, and S.M.Gubanski, "Dielectric mixtures: Electrical properties and modeling", IEEE Trans. Dielectric. Electr. Insul.,vol.9, no.5, pp. 809-828, Oct. 2002
5. Larry D. Smith, Raymond E. Anderson, Douglas W. Forehand, Thomas J. Pelc, and Tanmoy Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology", *IEEE Trans. On Advanced Packaging*, vol.33, no.3, August 1999
6. Y.W. Kim, J.H. Cho, K.Y. Kim, H.G. Kim, S. Sitaraman, V. Sundaram, R. Tummala and J.H. Kim, "Analysis and Optimization of a Power Distribution Network in 2.5D IC with Glass Interposer", *IEEE International 3D Systems Integration Conference,* Dec. 2014, Cork, Ireland.
7. H.G. Kim, H.S. Lee, J.H. Cho, Y.W. Kim and J.H Kim, "Electrical Design of Silicon, Glass and Organic Interposer Channels", *2014 Pan Pacific Microelectronics Symposium,* 2014, Kauaii, Hawaii, Feb.
8. J.Cho, Y.Kim and J.Kim, "Analysis of glass interposer PDN and proposal of PDN resonance suppression methods," *3D Systems Integration Conference (3DIC), 2013 IEEE International, Oct 2-5 2013*