

# Modeling, Design and Demonstration of Ultra-short and Ultra-fine Pitch Metastable Cu-Sn Interconnections with High-throughput SLID Assembly

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## Abstract

Advances in high-performance package with high I/O densities, and power modules with escalating current needs are driving the need for a new class of interconnection technologies, with thermal stability, current-carrying capability and pitch scalability beyond that of traditional solders. Solid-liquid interdiffusion (SLID or SoLID) or transient liquid phase (TLP) bonding systems, in which the bonding layer is fully converted to intermetallics, are highly sought after to extend the applicability of solders to pitches below 30 $\mu\text{m}$ , and for die-attachment in high-temperature high-power systems.

This paper introduces an innovative SLID concept, consisting of isolating a metastable intermetallic phase between barrier layers for a faster conversion to metastable composition than that in traditional SLID. The Cu-Sn system was used for this demonstration with a designed transition to metastable  $\text{Cu}_6\text{Sn}_5$  instead of the stable  $\text{Cu}_3\text{Sn}$  phase, usually targeted. The novel interconnection structure enables assembly within seconds and improved thermomechanical reliability, with all the benefits of SLID bonding such as outstanding thermal stability over 10x reflow and enhanced power handling capability with a current density of  $10^5 \text{ A/cm}^2$ . The paper first describes the design and fabrication of the interconnection structure, including the barrier and bonding layers based on diffusion and thermomechanical modeling. Ultra-fast assembly by low-pressure thermocompression bonding was demonstrated on die-attach joints and interconnections at 100 $\mu\text{m}$  pitch, followed by extensive reliability characterization, including thermal stability evaluation, electromigration test, and die-shear test. The designed interconnections successfully passed JEDEC standards, qualifying this novel interconnection technology for high-temperature, high-power operations at fine-pitch.

## 1. Introduction

High-performance systems are expected to drive interconnection pitches to 20 $\mu\text{m}$  and below in the next decade. The recent split-die trend, where a single large System-on-Chip (SOC) device is broken into two or four smaller dies which are then functionally reconstituted by high-density wiring on the substrate, further reinforces the need for ultra-fine-pitch interconnections. Pitch scaling is accompanied by shrinkage of the interconnections size, which requires a drastic reduction of solder volume in the standard Cu pillar

and solder cap technology. In this scope, massive intermetallics will cause serious reliability concerns.

Short interconnections with less than 10 $\mu\text{m}$  standoff height require low solder volumes in order to prevent bridging at fine-pitch. With standard solder-based interconnections, however, this raises serious reliability concerns, such as inferior power handling, increased stresses at the solder-intermetallic interfaces, and unstable joint compositions. All these including thermal stability, power-handling and minimum risk of bridging at fine-pitch require extending the applicability of solder-based interconnections to pitches below 30 $\mu\text{m}$ . The Georgia Tech approach is to extend SLID bonding or TLP bonding forming all-intermetallic interconnections of higher melting point. After the assembly, all the low melting point reactants will be completely consumed and replaced by high melting point resultant materials, which realizes the purpose of low-temperature assembly but high operating temperature capability [1].

SLID bonding has been shown to successfully overcome the limitations of solder and non-solder-based interconnection technologies, and also been highly sought after for die-attachment in power modules with operating temperatures exceeding 200 $^\circ\text{C}$ , especially for SiC diodes or MOSFETs, or GaN FETs [2]. Standard tin-based die-attach technologies used in Si power modules are qualified for 125 $^\circ\text{C}$  normal operations, but were shown to systematically fail beyond 250 $^\circ\text{C}$ , even with high-lead content [3,4]. Alternative technologies such as sintering of silver nanopastes have been extensively researched and implemented to some extent in commercial power modules, but the remaining porosity can degrade the electromigration performance [5,6]. On the other hand, outstanding thermal stability of Au-Sn SLID has been showed through 2000h high-temperature storage at 175 $^\circ\text{C}$ , and Cu-Sn SLID successively survived 30,000 power cycles when assembled onto DCB substrates [7,8]. However, further research is needed for new bonding technologies leading to high thermal, mechanical reliability and high throughput, also compatible with both fine-pitch applications and high-temperature die-attachment.

Various metallurgical systems have been studied such as Au-In, Ag-Sn, Au-Sn, Ni-Sn and Cu-Sn for SLID bonding. In Grummel's work, e-beam deposition and sputtering is required to form ultra-thin indium and gold layers, and bonding was performed in vacuum at 200 $^\circ\text{C}$  for 15minutes [9]. Subsequent phase transformation through multiple intermetallic compositions of Au-In after bonding was shown

with 150°C annealing, indicating unstable thermal properties [10]. For the Ag-Sn system, which is widely used in solar cells, lower transition rate and pores induced by volume shrinkage was reported [11,12]. High thermal stability and capability of withstanding CTE-mismatch of 25 ppm/K through HT-thermal cycling have been shown with Au-Sn SLID bonding. However, higher bonding temperature of 290°C to 350°C with dwell time exceeding 15minutes with continuous clamping pressure was necessary to form reliable joints, which limits applicability to HVM [13, 14]. Overall, the Cu-Sn SLID system has been identified as the most promising candidate, which can be fabricated with widely available processes without vacuum, be assembled at temperatures used for current soldering, and provides void-free joints.

The main challenges of current Cu-Sn SLID bonding are the low throughput from the long transition times to fully-stable intermetallics [15,16] and the reliability concerns due to inherent brittleness and accompanied Kirkendall voids [17]. Though several studies have shown that SLID interconnections can be formed within 1min by thermocompression bonding, the resulting constitution was still not completely stabilized. Further phase transformation could happen during subsequent high-temperature operations, raising reliability concerns. Non-ideal pores induced by volume shrinkage during intermetallics formation are also inevitable [18] without a comprehensive design of the SLID system.

In this paper, Cu<sub>6</sub>Sn<sub>5</sub> intermetallic is targeted as the final phase instead of the usual Cu<sub>3</sub>Sn. This is accomplished by introducing double-sided Ni(P) barrier layers that block the Cu source and suppress formation of Cu<sub>3</sub>Sn. Full transition to Cu<sub>6</sub>Sn<sub>5</sub> can be completely achieved through liquid-phase reaction with high throughput, while eliminating the subsequent solid-phase transition from Cu<sub>6</sub>Sn<sub>5</sub> to Cu<sub>3</sub>Sn. The key advantages of this technology are: a) high throughput assembly (<3s dwell time at peak temperature) compatible with standard thermocompression bonding tools and processes; b) ultra-thin (less than 5µm) bonding layers to prevent bridging at fine-pitch; c) higher thermal stability and electromigration resistance compared to traditional solder-based interconnections; and d) better thermomechanical reliability than state-of-the-art SLID technologies with lower standoff heights.

This paper demonstrates the metastable SLID bonding concept through design, fabrication, assembly and characterization. Finite element modeling was used to predict the interfacial stresses and strains to design the stack materials and geometries for improved reliability. Theoretical diffusion and kinetic models were used to optimize the thickness of the Ni barriers, the alternate Cu/Sn/Cu stack-up, and also the thermocompression bonding conditions. The designed stack-up with 2µm-thick Ni(P), 2µm-thick Sn and 1µm-thick Cu layers was successfully fabricated through precisely-controlled bump plating. An ultra-thin connecting layer below 5µm in thickness was achieved through high-throughput thermocompression bonding with 3s dwell time at 260°C. Outstanding thermal stability was shown through 10x reflows without any interfacial cracks or subsequent phase transformation. The power-handling capability was qualified

through electromigration test under high current density of 10<sup>5</sup> A/cm<sup>2</sup> at 150°C ambient temperature. Die-shear test with yielded specimens was conducted to provide quantitative evaluation of mechanical reliability.

## 2. Modeling and Design

### 2a. Metastable SLID Interconnection Design by Diffusion Model

The proposed metastable SLID bonding consisted of a joint made of Cu<sub>6</sub>Sn<sub>5</sub> intermetallics, isolated between Ni barrier layers. Diffusion and kinetic modeling were used to determine the thickness of both Ni(P) barrier layers and alternate Cu/Sn layers to achieve the targeted composition. Given the Cu/Ni/Cu<sub>6</sub>Sn<sub>5</sub> diffusion system, and the interdiffusion coefficients of Cu-Ni thin films reported [19], 27h is required for 0.1wt% Cu to diffuse through a 2µm-thick Ni barrier layer and reach the Ni/Cu<sub>6</sub>Sn<sub>5</sub> interface at 260°C. An extensive experimental study [20] also suggests that a 2µm-thick electroless Ni(P) layer can effectively prevent Cu diffusion after 2h of annealing at 400°C. Therefore, a 2µm electroless Ni(P) was considered as the diffusion barrier to inhibit further phase transformation from Cu<sub>6</sub>Sn<sub>5</sub> to Cu<sub>3</sub>Sn by successfully cutting off Cu supplies. The thickness of the Cu/Sn layers sandwiched between the barrier layers were calculated based on Equation (1) to accurately achieve the desired Cu<sub>6</sub>Sn<sub>5</sub> composition, in which *t* is the thickness of the plated layers, *M* is the atomic weight, and *ρ* is the elemental density. For the first concept demonstration, a symmetrical structure was evaluated, consisting of a 1µm-thick Cu and a 2µm-thick Sn layer, as shown in Fig. 1. Based on calculations, formation of a 5.4µm-thick layer of Cu<sub>6</sub>Sn<sub>5</sub> is expected by consumption of 4µm of Sn and 2µm of Cu.

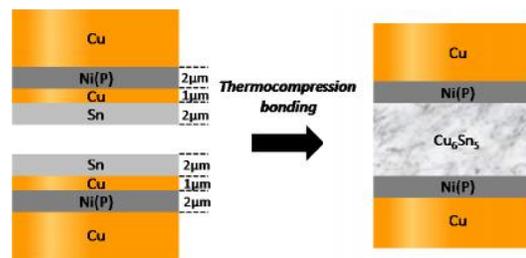


Fig. 1. Designed stack-up for metastable SLID bonding.

$$\frac{t_{Cu}}{t_{Sn}} = \frac{6M_{Cu}/\rho_{Cu}}{5M_{Sn}/\rho_{Sn}} \quad (1)$$

The kinetic model describing this liquid-phase reaction reported by Schaefer [21] was used to design the assembly process. A reaction time of 1min 20s is predicted at 260°C. For reference, traditional SLID bonding leading to a Cu<sub>3</sub>Sn composition requires a 20-30 minute transition time or post-annealing at high temperatures. As thermocompression bonding enhances interdiffusion, a shorter transition time is expected empirically.

2b. Thermomechanical Modeling for Design Optimization

Thermomechanical modeling was performed to further optimize the SLID stack-up design and compare the performance of the proposed SLID interconnection to the state-of-the-art Cu pillar with solder cap thermocompression bonding (TCB) technology. A finite element axisymmetric model of half of a single joint was built with ANSYS using 2D plane-183 elements. The detailed interconnection stack considered in this model is shown in Fig. 2. The test vehicle consists of a 600µm-thick die and a 100µm-thick substrate. In this study, silicon and FR-4 substrates were used, respectively, for 3D-IC applications and die-attach demonstration. For both TCB and SLID models, the structure includes a 2µm-thick Cu pad representing the routing layer and a 5µm-thick Cu pillar on the die side, and a 5µm-thick Cu trace on the substrate side forming the landing pad. Ni(P) layers are considered on bumps and substrates as barrier layers, and to emulate the standard ENIG or ENEPIG surface finish in the latter case. The thickness of the connecting layer sandwiched between two barrier layers was defined as the summation of intermetallics and residual solder in the TCB case, but as the thickness of intermetallics only in the SLID case. Isotropic material properties were assumed for most of the structure materials, as shown in Table 1. Plasticity of copper was represented with a bilinear kinematic hardening model as shown in Table 2. Anand’s viscoplastic model was used for the Sn3.5Ag solder, with parameters reported in Table 3. The boundary condition was applied by setting the reference temperature to 150°C and cooling down to room temperature to capture the temperature drop in assembly. Mesh convergence was confirmed by refinement of the mesh size.

Interfacial stresses are the principal cause of failure in such interconnections, due to the large difference in mechanical properties between brittle and ductile materials considered in the interconnection stack. The Von-Mises stress concentrated at the interface between intermetallics (Cu<sub>6</sub>Sn<sub>5</sub>) and solder (Sn3.5Ag) as a function of the connecting height is shown in Fig. 3. Interfacial stress dramatically increases for bump heights below 13µm. The standard TCB structure is much more sensitive to reductions in standoff height as confirmed by the larger slope due to wider discrepancies in the material properties of solder, Ni, Cu and Cu<sub>6</sub>Sn<sub>5</sub>. The adhesion strength between Cu-Sn intermetallics and solder is reported to be in the 50-81.3 MPa range [22,23]. The SLID structure brings less interfacial stress, and thus less risk of cracking than its solder counterpart when considering ultra-short bumps, for both silicon and organic substrates.

In a CTE-matched Si-to-Si structure, both TCB and SLID interconnections have interfacial stresses below 100 MPa, indicating promising reliability. However, when introducing CTE mismatch, the traditional TCB interconnections present risks of failure due to highly-concentrated stresses, while the SLID interconnections provide a more reliable alternative.

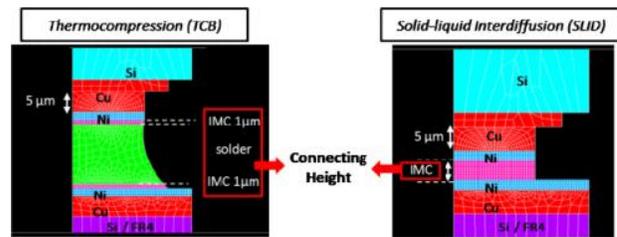


Fig. 2. ANSYS models built for TCB and SLID interconnections.

Table 1. Isotropic material properties

Materials	Silicon	Nickel	Cu <sub>6</sub> Sn <sub>5</sub>	FR-4
E(GPa)	129.85	200	112.3	23.4
Poisson’s ratio	0.28	0.3	0.3	0.136
CTE (ppm/K)	2.56	13.4	16.3	17.4

Table 2. Bilinear kinematic hardening model for copper

Parameters	Value
E(GPa)	121
Poisson’s ratio	0.3
Initial yield stress (MPa)	172.38
Tangent modulus (MPa)	1034.2

Table 3. Anand’s viscoplastic model parameters for Sn3.5Ag

Parameters	Value	Parameters	Value
So (MPa)	42.09	H <sub>0</sub> (MPa)	3521.5
Q/R (K)	10279	M	0.207
A	177016	n	0.0177
X <sub>i</sub>	7	a	1.6
S <sub>h</sub> (MPa)	52.4		

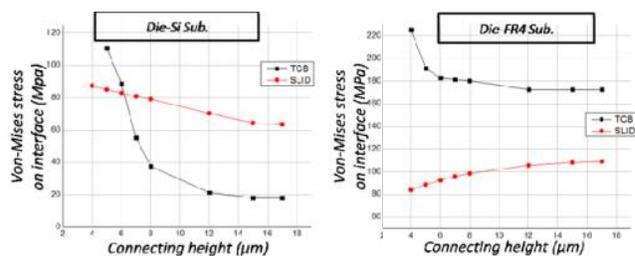
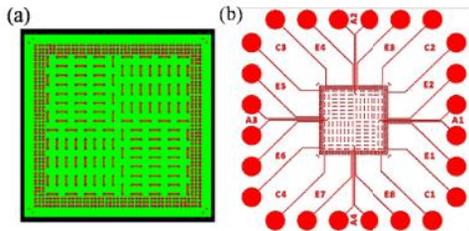


Fig. 3. Interfacial Von-Mises stress as a function of the standoff height of the TCB and SLID structures, bonded on Si or FR-4 substrates.

### 3. Test Vehicle Fabrication

To prove the applicability and robustness of this technology for both die-attach power applications and fine-pitch off-chip interconnections, two test vehicles were fabricated. The first one emulates a die-attach configuration for power modules, where DBC substrates are typical. The interconnection introduced in Fig. 1 was fabricated on a 1mm-thick Cu-clad FR-4 substrate, in a blanket-type structure with large connecting area. The second test vehicle was built on a 600 $\mu\text{m}$ -thick silicon wafer with daisy chain structures at 100 $\mu\text{m}$  pitch, which provides the electrical measurement capability for reliability tests of thermal stability and power handling. Fig. 4 shows the electrical design of the test vehicle which contains 760 I/Os, with three peripheral rows at 100 $\mu\text{m}$  pitch and a central area array at 250 $\mu\text{m}$  pitch.

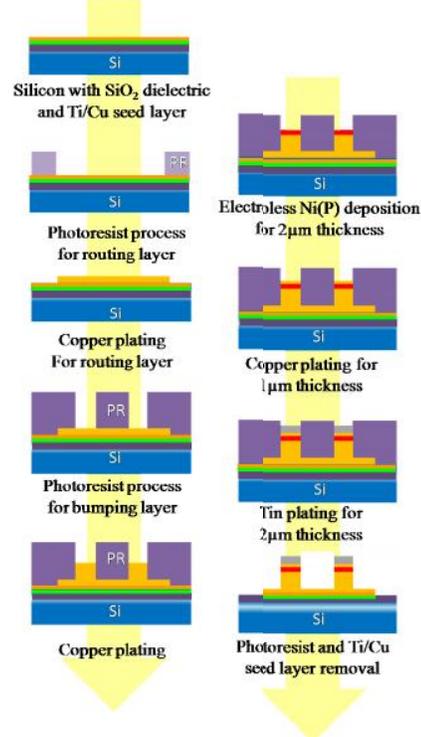


**Fig. 4.** Electrical designs of (a) daisy-chain die, and (b) substrate.

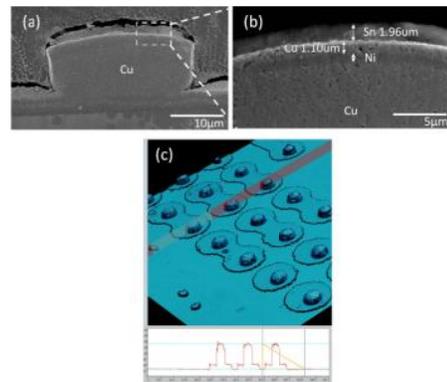
A two-step photo-lithography process was used for wafer fabrication, following the process flow presented in Fig. 5. The 15 $\mu\text{m}$ -thick Hitachi RY-5315EB dry-film photoresist and 25 $\mu\text{m}$ -thick Hitachi Sample A dry-film were used for patterning of the routing and bump layers, respectively. Development was performed with a 3%  $\text{Na}_2\text{CO}_3$  solution at 85 $^\circ\text{C}$ , followed by plasma etching to remove the residual organics that could contaminate the opened area. The Cupracid TP and Stannobond FC chemistries were used for copper and tin electrolytic plating, and the Ni(P) barrier layer was plated with the electroless Aurotech CNN chemical. A current density of 2 ASD was first used for Cu deposition to form the routing and bump layers. After Ni(P) electroless plating, lower plating rates of 0.75 ASD and 1ASD were used for copper and tin plating, respectively, in order to control the plated thickness more accurately. Through the whole process, the thickness could be well-controlled via the dipping or plating time. The Enthone PC 4025 stripper solution was then used to strip the photoresist, and the Cu/Ti seed layer was etched by Transcene Copper Etchant 49-1 and plasma etching.

Figs. 6(a, b) shows the backscattered electron images (BEI) of the fabricated stack-up which is composed of 1.72 $\mu\text{m}$  Ni(P) barrier, 1.1 $\mu\text{m}$  Cu and 1.96 $\mu\text{m}$  Sn. Processing errors for the respective layers are 14%, 10% and 2% with respect to the designed thickness. Since SLID bonding targets intermetallics only that hold exact elemental ratios with limited composition deviation, accurate thickness control is critical. An excessive Cu supply would turn the metastable SLID interconnections back into its traditional form of  $\text{Cu}_3\text{Sn}$ , in which massive Kirkendall voids and shrinking pores cannot be avoided. In the event of excessive Sn, residual solder would also degrade the thermal stability and power handling

of the formed interconnections. Micro-cracks propagating through the interface are then to be expected according to the previous finite element modeling results. X-ray energy dispersive spectroscopy (XEDS) analysis shows 7.6-9.84 at% phosphorus in the Ni(P) layer without any findings of  $\text{Ni}_3\text{P}$  crystalline in the as-plated state. The bumps coplanarity was evaluated by confocal microscopy using the Olympus LEXT 3D Material, illustrated in Fig. 6(c). The bump height ranged from 11.84 $\mu\text{m}$  to 12.16 $\mu\text{m}$ , indicating a 6.21% height variation within one 5mm x 5mm die. Without the bulk of solder that is used to accommodate this height variation, highly required coplanarity is one of the challenges of using ultra-thin connecting layers.



**Fig. 5.** Process flow for fabrication of designed metastable SLID interconnection stack-up.



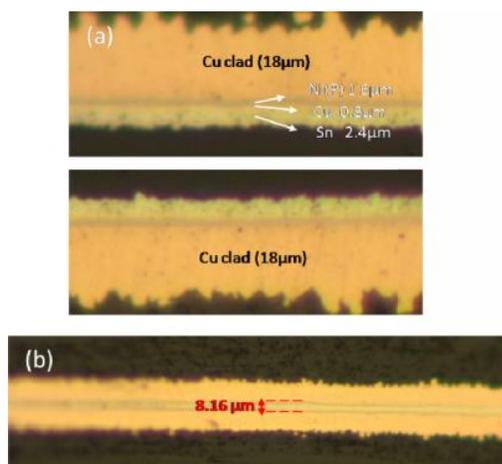
**Fig.6.** (a) Backscattered electron images (BEI) of a plated bump, (b) The Ni(P)/Cu/Sn multi-layered structure, and (c) 3D confocal microscopy image of plated bumps on a 5mmx5mm die.

## 4. Assembly and Evaluation of Composition and Strength

### 4a. Assembly Process

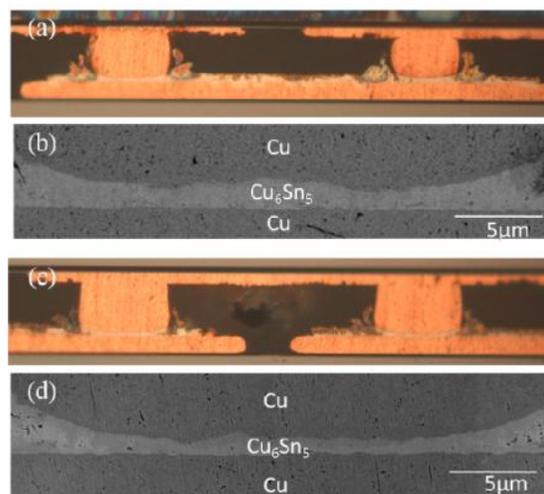
Assembly was performed by thermocompression bonding using a semi-automatic Finetech Fineplacer Matrix flip-chip bonder with a placement accuracy of  $\pm 3\mu\text{m}$ . The first demonstration was conducted on the 5mmx5mm blanket-like structure of Fig. 7(a), fabricated on a 1mm-thick Cu-clad organic substrate to emulate large-area die-attachment. The samples were bonded at 260°C with a 3.2MPa applied pressure and a 1 min dwell time at peak temperature. A 20% variation was observed in the plating thicknesses. A well-connected interface was achieved across the whole 5mm x 5mm area as confirmed by the cross-section pictures in Fig. 7(b). XEDS analysis confirmed the  $\text{Cu}_6\text{Sn}_5$  composition, verifying the metastable SLID bonding concept.

Applicability of the proposed technology for off-chip interconnections was demonstrated with the second test vehicle with a daisy chain design at 100 $\mu\text{m}$  minimum pitch. A pre-applied epoxy-based B-stageable no-flow underfill without fillers (BNUF by Namics Corporation) was used for this study to control the bump shape and lateral spreading under thermocompression. The material is dispensed on the bonding site of the substrate and B-staged at 70°C for 1h. Assembly was performed at 260°C for 1min with an applied pressure of 40MPa, required to ensure bump-to-pad contact through the underfill layer. Cross-section images of the bonded samples are shown in Figs. 8(a, b). Void-free interconnections composed of only  $\text{Cu}_6\text{Sn}_5$  were successfully achieved without any trace of  $\text{Cu}_3\text{Sn}$ . To further improve the assembly throughput and manufacturability of the metastable interconnection, a two-step process is proposed with first thermocompression bonding with a 3s dwell time to initiate the reaction, followed by a standard reflow cycle for full transition into intermetallics that could be completed during board-level assembly with a standard SMT process. As shown in Figs. 8(c, d), metastable SLID joints made of  $\text{Cu}_6\text{Sn}_5$  were successfully formed by this two-step assembly process. Perfect yield has been achieved in all the cross-sectioned specimens according to electrical measurement.



**Fig.7.** Cross-sections of (a) the stack-plated structure on a copper clad FR-4 substrate before assembly, and (b) an assembled 5mmx5mm blanket-like sample, formed by thermocompression bonding at 260°C, 3.2MPa, 1min.

The transition time is considerably shortened comparing to the typical 20-30 minute required to achieve the ultimate stable phase  $\text{Cu}_3\text{Sn}$  in the state-of-the-art Cu-Sn SLID, which can be well explained by the interfacial reactions between Cu and Sn. While forming  $\text{Cu}_6\text{Sn}_5$  ( $\eta$ ), the growth rate is dominated by the dissolution of Cu into molten solder, precipitation of  $\text{Cu}_6\text{Sn}_5$  and ripening of scalloped  $\text{Cu}_6\text{Sn}_5$ . The whole transition can be completed through liquid-state reaction and the grain boundary diffusion through neighboring  $\text{Cu}_6\text{Sn}_5$ , massive  $\text{Cu}_6\text{Sn}_5$  thus was expected to grow within several seconds [24]. On the contrary, the formation of  $\text{Cu}_3\text{Sn}$  ( $\epsilon$ ) requires solid-state reactions between  $\text{Cu}_6\text{Sn}_5$  and Cu at the interface, in which molten solder is not involved. As it is controlled by grain boundary diffusion of Cu through  $\text{Cu}_6\text{Sn}_5$ , full transition from  $\text{Cu}_6\text{Sn}_5$  into  $\text{Cu}_3\text{Sn}$  generally takes several hours [25]. As indicated in Fig. 1,  $\text{Cu}_6\text{Sn}_5$  is directly in contact with the Ni(P) barrier layers. Subsequent phase transformation into  $(\text{Ni}_{1-x}, \text{Cu}_x)_3\text{Sn}$  or  $(\text{Ni}_{1-x}, \text{Cu}_x)_3\text{Sn}_4$  would be possible if a massive Ni supply is available. However, from a thermodynamic standpoint, the SnCuNi ternary phase diagram indicates that  $\text{Cu}_6\text{Sn}_5$  can accommodate 32 at% of Ni substitution in the form of  $(\text{Ni}_{0.59}\text{Cu}_{0.41})_6\text{Sn}_5$  [26]. Addition of Ni into the solder on the other hand further stabilizes  $(\text{Ni}_x\text{Cu}_{1-x})_6\text{Sn}_5$  and accelerates the growth rate of  $(\text{Ni}_x\text{Cu}_{1-x})_6\text{Sn}_5$  [27], which enhances the transition rate of metastable SLID interconnections. From the kinetic viewpoint, comparatively slow diffusivity of Ni in  $\text{Cu}_6\text{Sn}_5$  ranged from  $10^{-18}$  to  $10^{-19}$   $\text{m}^2/\text{s}$ , also interferes further phase transformation [28].



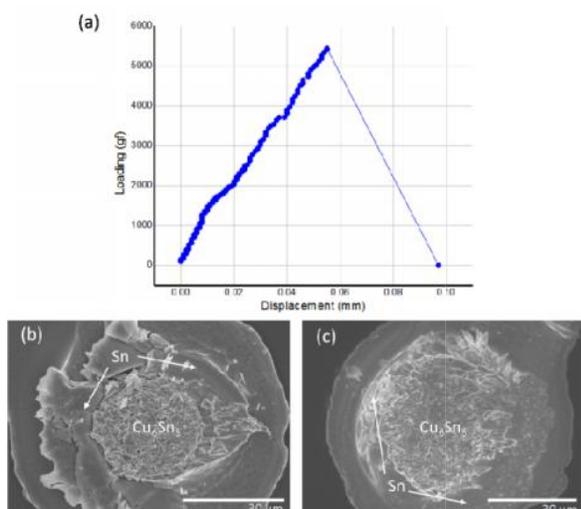
**Fig.8.** Optical and SEM images of cross-sections of assembled metastable SLID interconnections (a, b) by thermocompression bonding at 260°C, 40MPa with a 1min dwell time; and (c, d) by a 2-step process with 3s thermocompression and subsequent reflow.

### 4b. Die-Shear Test

Daisy-chain samples were assembled without pre-applied underfill to quantify the quality of the joints through die-shear testing. The assemblies were formed by 1min thermocompression bonding at 260°C with an applied pressure of 10MPa to compensate for bumps non-coplanarities. Die-shear test was carried out following the MIL-STD-883G Method 2019.7, which is used for bonding

strength evaluation of die-attach technologies. For a die size of  $25\text{mm}^2$ , the minimum force required to pass this standard is of 2.5 kgf, or 6MPa with considerations of the total bonded area that actually contributes to the overall strength. A Dage-Series-400 bond tester was used for this evaluation, with a die-shear cartridge of 10 kgf. The speed of the shear tool was set to  $32.0\mu\text{m/s}$ , and the tool height was  $5\mu\text{m}$  which was defined as the distance from the tip of the contact tool to the top of the substrate. Shear strength values in MPa were derived from the maximal loading measured (kgf) before failure.

The shear strength measured for the 4 tested samples were of 4.4kgf, 5.5 kgf, 4.6kgf and 5.1kgf, which corresponds to shear strengths in the 81-93MPa range. The shear profile with the maximal loading of 5.5 kgf is shown in Fig. 9(a). On average, the shear strength was found to be 90 MPa which is more than 10x the minimum MIL-standard, with a standard deviation of 8.4 MPa. Shear strength values around 40 MPa were reported for traditional Cu-Sn SLID bonding [29], indicating a significant improvement of the bonding strength with  $\text{Cu}_6\text{Sn}_5$  SLID interconnections. Die-shear failures in traditional Cu-Sn SLID bonding typically occur at the interface between  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  or within the  $\text{Cu}_3\text{Sn}$  layer due to Kirkendall voids. The strengths of these weakest layers cause the bonding strength of state-of-the-art Cu-Sn SLID lower than 40MPa [22]. In the case of metastable SLID bonding, brittle fracture happened through the bulk of the void-free  $\text{Cu}_6\text{Sn}_5$  layer, as confirmed in Figs. 9(b, c) by the presence of  $\text{Cu}_6\text{Sn}_5$  on both die side and substrate sides. Consequently, the high fracture strength of  $\text{Cu}_6\text{Sn}_5$  contributed to the enhanced bonding strength of the metastable SLID interconnections. No  $\text{Cu}_3\text{Sn}$  or Ni/Cu layers were found on the fracture surface through XEDS analysis, which further indicates the design of metastable SLID bonding can successfully inhibit the growth of  $\text{Cu}_3\text{Sn}$ .

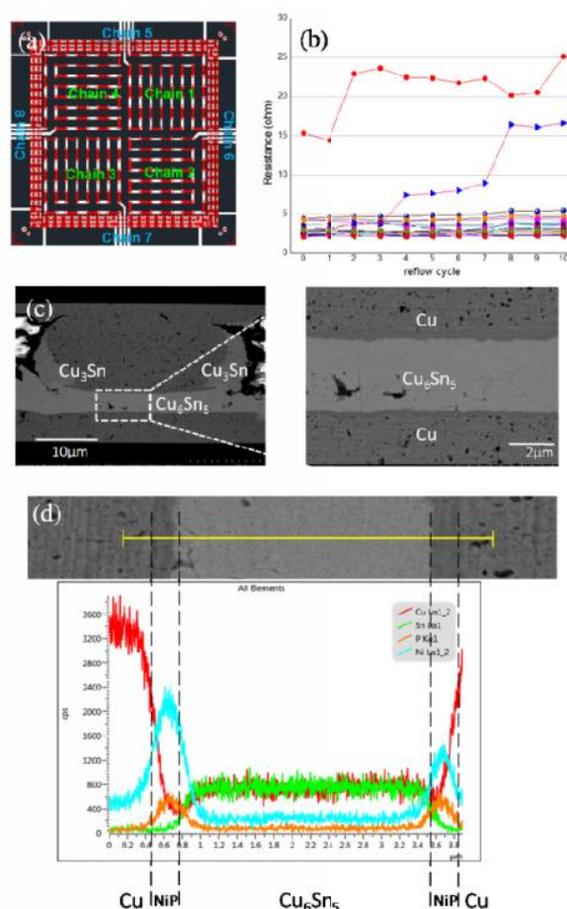


**Fig.9.** (a) Shear test profile of one of four test samples; SEM images of the fracture surface, (b) of the bumps on die side, and (c) on the substrate side.

## 5. Reliability Characterization

### 5a. Thermal Stability Evaluation

The thermal stability of the metastable SLID interconnection was assessed by monitoring the daisy chain resistances values over a 10x reflow accelerated test, performed in a reflow oven at  $260^\circ\text{C}$  peak temperature. Test vehicle containing eight daisy chains was used as shown in Fig. 10(a). The resistances measured after each reflow cycle are plotted in Fig. 10(b), with 22 out of 24 daisy chains that survived this multiple reflow test. The non-coplanarities of bumps might be responsible for the observed early failures. The BEI images and corresponding XEDS line scans taken on cross-sections of assembled parts after 10x reflow are shown in Figs. 10(c, d), respectively. The Ni(P) barrier layers remained intact even after multiple reflows, the intermetallics between Cu bumps and landing pads were confirmed as  $\text{Cu}_6\text{Sn}_5$  by XEDS.



**Fig. 10.** (a) Electrical design of the test vehicle with separate corner, side and center daisy chains, (b) Resistance measurements of the 24 daisy chains through 10x reflow, (c) BEI of metastable SLID interconnections after 10x reflow, and (d) XEDS line scan across the connecting layer.

To further understand the Ni consumption through 10x reflow, Dybkov's analysis which describes copper consumption into molten tin is used as shown in Equation (2), in which  $C_s$  is the solubility of copper in the molten tin,  $C$  is

the concentration of copper in the molten tin,  $S$  is the surface area of copper,  $V$  is the volume of the molten tin, and  $k$  is a constant [30]. The Ni(P)/Cu<sub>6</sub>Sn<sub>5</sub> diffusion couple is considered in this study,  $C_s$  can be regarded as the solubility of Ni in Cu<sub>6</sub>Sn<sub>5</sub>,  $C$  is the concentration of Ni in the Cu<sub>6</sub>Sn<sub>5</sub>, and the constant  $k$  should also be proportional to the diffusivity of Ni through Cu<sub>6</sub>Sn<sub>5</sub>.

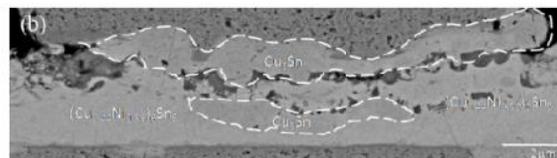
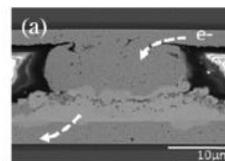
$$\frac{dc}{dt} = k \frac{S}{V} (c_s - c) \quad (2)$$

Considering the diffusivity of Ni through Cu<sub>6</sub>Sn<sub>5</sub> reported in the literature, substitution of Cu<sub>6</sub>Sn<sub>5</sub> by 10 at% Ni would take more than 50h at 260°C, a much longer duration than the 10x reflow test. Since the dissolution rate is also proportional to the diffusivity, the dissolution of Ni into Cu<sub>6</sub>Sn<sub>5</sub> was also interfered by the decreasing diffusivity of Ni in Cu<sub>6</sub>Sn<sub>5</sub> with increasing Ni content. This accelerated multiple-reflow test thus proves the outstanding thermal stability of the metastable SLID structure, which is ideal for die-stacking application in 3D IC and 3D integrated power modules.

### 5b. Electromigration Test

Considering the fundamental equation of critical product which describes the stress balance between current stressing and backward mechanical stress [31], assuming that ideal Cu-Cu interconnections can handle a 10<sup>6</sup> A/cm<sup>2</sup> current density as several studies have previously demonstrated, traditional solder-caped interconnections can only sustain a 3x10<sup>3</sup> A/cm<sup>2</sup> current density, while SLID interconnections are projected a higher power handling capability, withstanding a 5x10<sup>4</sup> A/cm<sup>2</sup> current density. Therefore, the electromigration test was carried out with a current density of 10<sup>5</sup> A/cm<sup>2</sup> at 150°C ambient temperature, to benchmark against traditional solder-based interconnections.

SEM/XEDS analysis presented in Figs. 11(a, b), shows that the Ni(P) layer and Cu bump were partially dissolved into Cu<sub>6</sub>Sn<sub>5</sub> at the cathode while the Ni(P) layer remained intact at the anode after 500h. This UBM consumption induced by current stressing has been reported before in the case of traditional solder joints [32], where the Cu and Ni from the cathode react, forming Cu<sub>3</sub>Sn and (Ni<sub>0.56</sub> Cu<sub>0.44</sub>)<sub>6</sub>Sn<sub>5</sub> within the connecting layer. Voids and microcracks distributed along the interface between Cu<sub>3</sub>Sn and (Ni<sub>0.56</sub> Cu<sub>0.44</sub>)<sub>6</sub>Sn<sub>5</sub> were mainly found near the cathode interface, similarly to the classical pancake-like void failure reported in previous electromigration studies [33]. These voids may be attributed to the differential mass transportation rates between Cu<sub>3</sub>Sn and (Ni<sub>0.56</sub> Cu<sub>0.44</sub>)<sub>6</sub>Sn<sub>5</sub> under current stressing. Ideal power handling capability up to 1000h of current stressing can be achieved with further optimization of the Ni(P) barrier thickness and composition.



**Fig.11.** (a) BEI of a single joint after 500h of current stressing with a current density of 10<sup>5</sup> A/cm<sup>2</sup>, and (b) Distribution of intermetallics within the connecting layer.

## 6. Conclusions

In this study, a new concept of metastable SLID interconnections was demonstrated for the first time with the Cu-Sn system. The interconnection structure was designed based on mechanical and kinetic modeling. The ultimate targeted composition was the metastable Cu<sub>6</sub>Sn<sub>5</sub> intermetallic instead of the typical Cu<sub>3</sub>Sn, which enables a 10x reduction in transition time for shorter assembly cycle times. A two-step assembly process was demonstrated, where the reaction is initiated during a 3s thermocompression bonding, then completed during subsequent reflow for board-level processing. The novel metastable interconnections showed outstanding thermal stability through 10x reflow, in which no further phase transformation was observed due to the effectiveness of the Ni(P) barrier layers. Results from electromigration test with a 10<sup>5</sup> A/cm<sup>2</sup> current density show the promising potential of this metastable SLID approach in handling ultra-high current density beyond the capability of traditional solder. Die-shear strength experiments were also conclusive with an average bonding strength of 90MPa, which confirms the excellent mechanical reliability of the formed joints. Metastable SLID bonding thus constitutes a promising alternative for next-generation solder-based interconnections. This technology can be applied to ultra-thin and ultra-short 3D ICs, off-chip interconnections, and power devices with high current-handling capabilities.

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## References

- [1] W.D. MacDonald, T.W. Eagar, *Annu. Rev. Mater. Sci.* 22 (1992), 23-46.
- [2] M. Ostling, R. Ghandi, C.M. Zetterling, *Proceedings of the 23<sup>rd</sup> International Symposium on Power Semiconductor Devices & IC's* (2011), 10-15.

- [3] P. Ning, Z. Liang, F. Wang, L. Marlino, *Applied Power Electronics Conference and Exposition (APEC)*, Twenty-Seventh Annual IEEE (2012), 2134-2139.
- [4] L. Coppola, D. Huff, F. Wang, R. Burgos, D. Boroyevich, *Power Electronics Specialists Conference (PESC)* (2007), 2234-2240.
- [5] J.G. Bai, Z. Zhang, J.N. Calata, G.Q. Lu, *IEEE Trans. Compon. Packag. Technol.* 29 (2006), 589-593.
- [6] T.G. Lei, J.N. Calata, G.Q. Lu, *IEEE Trans. Compon. Packag. Technol.* 33 (2010), 98-104.
- [7] N. Heuck, K. Guth, M. Thoben, A. Muller, N. Oeschler, L. Bower, R. Speckels, S. Krasel, A. Ciliox, *Integrated Power Electronic Systems Conference* (2014), 1-6.
- [8] K. Guth, N. Oeschler, L. Bower, R. Speckels, G. Strotmann, N. Heuck, S. Krasel, A. Ciliox, *Integrated Power Electronics Systems Conference* (2012), 1-5.
- [9] B.J. Grummel, Z.J. Shen, H.A. Mustain, A.R. Hefner, *IEEE Trans. Compon. Packag. Technol.* 3 (2013), 716-723.
- [10] L. Deillon, T. Hessler, A. Hessler-Wyser, M. Rappaz, *Acta Mater.* 79 (2014), 258-267.
- [11] J.F. Li, P.A. Agyakwa, C.M. Johnson, *Acta Mater.* 58 (2010), 3429-2443.
- [12] A. Lis, M.S. Park, R. Arroyave, C. Leinencach, *J. Alloys Compd.* 617 (2014), 763-773.
- [13] T.A. Tollefsen, A. Larsson, O.M. Lovvik, K. Aasmundtveit, *Metall. Mater. Trans. B* (2012), 397-405.
- [14] T.A. Tollefsen, A. Larsson, O.M. Lovvik, K. Aasmundtveit, *IEEE Trans. Compon. Packag. Technol.* 3 (2013), 904-914.
- [15] H. Liu, K. Wang, K.E. Aasmundtveit, N. Hoivik, *J. Electron. Mater.* 41 (2012), 2453-2462.
- [16] K. Tanida, M. Umamoto, N. Tanaka, Y. Tomita, K. Takahashi, *Jpn. J. Appl. Phys.* 43 (2004), 2264-2270.
- [17] K. Zeng, R. Stierman, T.C. Chiu, D. Edwards, K. Ano, K.N. Tu, *J. Appl. Phys.* 97 (2005), 024508.
- [18] H.Y. Chuang, T.L. Yang, M.S. Kuo, Y.J. Chen, J.J. Yu, C. C. Li, C. R. Kao, *IEEE T. Device Mat. Re.* 12 (1988), 155-160.
- [19] R. Venos, W. Pamler, H. Hoffmann, *Thin Solid Films* 162 (1988), 155-160.
- [20] E.J. O'sullivan, A.G. Schrott, M. Paunovic, C.J. Sambucetti, J.R. Marino, R.J. Bailey, S. Kaja, K.W. Semkow, *IBM J. RES. DEVELOP* 42 (1998), 607-620.
- [21] M. Schaefer, R.A. Fournelle, J. Liang, *J. Electron. Mater.* 27 (1998), 1168-1176.
- [22] I. Panchenko, J. Grafe, M. Mueller, K.J. Wolter, *Electronic System Integration Technology Conference* (2012), 1-7.
- [23] H.T. Lee, M.H. Chen, *Mater. Sci. Eng. A.* (2002), 24-34.
- [24] H.K. Kim, K.N. Tu, *Phys. Rev. B* 53 (1996), 16027-16034.
- [25] R.A. Gagliano, M.E. Fine, *J. Electron. Mater.* 32 (2003), 1441-1447.
- [26] C.Y. Li, G.J. Chiou, J.G. Duh, *J. Electron. Mater.* 35 (2006), 343-352.
- [27] Y.W. Wang, Y.W. Lin, C.T. Tu, C.R. Kao, *J. Alloys Compd.* 478 (2009), 121-127.
- [28] K.C. Huang, F.S. Shieu, Y.H. Hsiao, C.Y. Liu, *J. Electron. Mater.* 41 (2012), 172-175.
- [29] K.E. Aasmundtveit, T.T. Luu, A.B. Vardoy, T.A. Tollefsen, K. Wang, N. Hoivik, *Electronics System-Integration Technology Conference* (2014), 1-6.
- [30] M.L. Huang, T. Loeher, A. Ostmann, H. Reichl, *Appl. Phys. Lett.* 86 (2005), 181908.
- [31] K.N. Tu, *J. Appl. Phys.* (2003), 5451-5473.
- [32] Y.H. Lin, C.M. Tasi, Y.C. Hu, Y.L. Lin, C.R. Kao, *J. Electron. Mater.* 34 (2005), 27-33.
- [33] Y. Yao, L.M. Keer, M.E. Fine, *J. Appl. Phys.* 105 (2009), 063710.