Modeling, Design and Demonstration of Ultra-miniaturized Glass PA Modules with Efficient Thermal Dissipation

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Abstract

This paper addresses the thermal dissipation of power amplifier (PA) chips, which is one of the biggest challenges in the development of ultra-miniaturized glass-based RF modules. Glass packages with 3D or double-side active and passive integration offer the best miniaturization and performance enhancement for RF modules because glass has ultra-low loss, dimensional stability for precision thinfilm components, ability to process through-vias in large panels to reduce cost [1]. However, glass is a poor thermal conductor. Cooling of the high-power PA die with integrated miniaturized RF modules is, therefore, a key challenge. This paper provides extensive modeling studies of RF power amplifier modules with copper thermal vias in ultra-miniaturized glass, without additional process steps. It considers various power amplifier design options such as: a) Si vs. Silicon-on-Insulator (SOI), b) location of die hotspot, c) via geometry, and d) conformal vs. fully-filled vias, and provides optimal design recommendations with modeling and analysis.

Introduction

Glass package technology in 2D, 2.5D and 3D is emerging as an ideal solution for high-performance and ultra-miniaturized RF modules with simultaneous reduction in both X-Y and Z directions. This is because glass provides many advantages such as, ultra-thinness, ultra-low electrical loss, silicon-like dimensional stability, high stiffness, high Tg, high surface smoothness and adjustable coefficient of thermal expansion (CTE) [2]. It is superior to silicon for RF applications because it enables high-Q RF components. Compared to organics, glass enables precision component design with finer design ground rules because of its dimensional stability, and ability to process with ultra-thin and low-loss build-up organic or inorganic dielectrics, without process-compatibility issues. Recent advances at Georgia Tech PRC have demonstrated reliable and fine-pitch through-vias in glass double-side assembly of active and passive components with ultra-short interconnections [3]. In addition to these, glass as a packaging substrate appears to be a perfect solution for its cost effectiveness. However, glass has two major challenges: brittleness and low thermal conductivity. This paper addresses the second challenge by creating high-density and low-cost copper vias inside the glass for efficient cross-plane thermal conduction. Glass substrates with through-package-vias (TPVs) are expected to offer unique opportunities not only with enhanced RF performance and reliability but also with low cost. [4].

An RF PA converts a low-power RF signal into a high-power signal, typically for driving the antenna of a transmitter. However, even an RF PA with a very good power efficiency utilizes less than half of the total power supplied. More than 60% of the supplied power is dissipated as heat, depending on the PA design. With the trend toward increased miniaturization with higher component densities, the heat dissipation of PA becomes a major bottleneck for RF performance and reliability. As the power density, or the rate of heat dissipated per unit area across the chip further escalates, the performance of sensitive components such as matching networks that are in proximity with the PA die also get affected. Therefore, more effective ways to dissipate the heat from the PA die through the package and down to the printed circuit board (PCB) need to be developed.

Several solutions are being explored for thermal management of high-power density RF devices. These include passive cooling techniques such as heat pipes and heat sinks, or active techniques involving cooling fans, microfluidic channels and even spray cooling.

Heat pipes utilize evaporation and condensation to achieve a much higher effective thermal conductivity. In a detailed analysis by Langari et al., almost 26% decrease in maximum junction temperature was achieved with such cooling techniques [5]. Alternative techniques such as passive heat sinks are also commonly used depending on thermal budget and external conditions surrounding the chip [6].

In high-power applications such as in processors and servers, cooling fans [7] are commonly used in combination with heat sinks to augment heat-transfer. Microfluidic cooling [8] is another convective heat transfer technology where water flows in a closed loop underneath the chip for heat removal. A recent analysis by Wan et al. showed a temperature drop of 18.8°C and 66.2% reduction in leakage current with microfluidic cooling compared to natural air cooling, at a heat flux of 34.5 W/cm^2. In spray cooling methods [9], these systems contain micro-machined nozzles, which inject a constant flow of fluid, at ~0.15 l/min, onto the heated RF PA die. With this approach, the junction temperature and the total thermal resistance were estimated to reduce from 214°C to 115°C, and from 1.5°C/W to 0.6°C/W respectively.

In RF power amplifier modules, which is the key focus of this paper, three options are widely pursued for chip cooling. These are over-molded plastic (OMP) packaging, phase change materials (PCM), and active heat sinks. To improve the thermal performance and electrical grounding, Nelson at el. [10] considered several factors such as materials selection, mechanical design parameters, assembly materials, and inspection tools for reliable solder joints with low thermal resistance. In a detailed parametric study, the heat-dissipation

characteristics of different heat sink materials such as copper and aluminum are also compared. These results demonstrate the superiority of copper for heat dissipation. In addition the drop in junction temperature by about 10°C to 20°C caused a doubling of the mean-time-to-failure (MTTF). Another technique is the introduction of a heat-capacitor such as PCM, which absorbs heat through a phase transition in the material. Hoffman et al. [11] performed a detailed thermal analysis with several materials and studied their locational variation. Eicosane paraffin wax was used as PCM because of its high latent heat capacity and melting point of 36°C. The latent heat storage of the PCM was experimentally determined to be 50.5kJ/kg, which is higher than the design specification of 48.7kJ/kg in the paper. Thus, during the phase transition region, the module was able to maintain a constant temperature at 48°C, over defined periods of continuous operation for up to 30 min. Lastly, another approach, based on active heat sink antenna [12] utilizes the antenna for multiple purposes; not only utilizing it as a transmitter but also for cooling. In the suggested structure, the PA circuit is connected to the wire-fed patch antenna by a conducting cylinder, which acts as a heat spreader to the ground plane.

This paper addresses the PA thermal dissipation challenge with ultra-miniaturized glass packages without the need for additional passive and active cooling structures and processes. This is accomplished with low-cost copper through-vias to effectively dissipate the heat from the PA hotspot, as illustrated in Fig. 1. Georgia Tech and its partners have shown that glass interposers and packages can be fabricated with ultra-high-density copper TPVs with low-cost processes [3].The Cu TPV-based cooling was previously applied to glass interposers by Cho et al. [4]. This paper applies this concept to RF PA modules. The key performance parameters and targets for the modules are shown in Table 1.

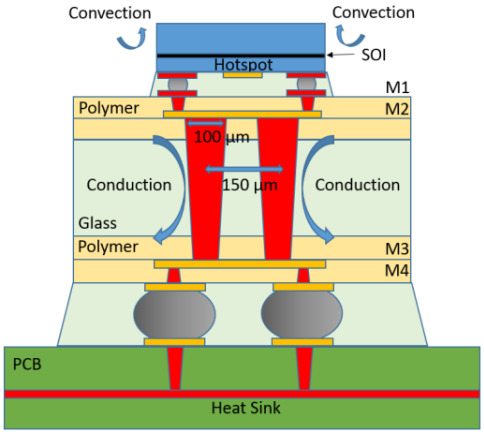

Fig. 1. RF PA Module with thermal via structures for effective heat dissipation.

Table 1. PA module parameters and targets

Power	1W
Power Efficiency of PA	30%
PA Die Size	3.5mm x 2.5mm
Hot Spot Size (10% of Die Size)	350µm x 250µm
Junction Temperature	185°C
Target Die Steady State Temperature	85°C

Modeling

A detailed thermal model for cooling PA chips with different thermal via designs was setup using the commercial package COMSOL. The model simulates heat transfer from the PA die that is flip-chip assembled with solder or copper bumps with blind vias on the build-up layers, with glass TPVs, and then onto the PCB. Different boundary conditions for hotspots where considered. These involve PA with cooling from both top and bottom sides through convection, silicon-on-insulator (SOI) with an oxide thickness of 1µm between the active device layer and the silicon which allows heat transfer predominantly from the bottom side using thermal vias, and different hot-spot locations on PA (die edge or die center), Structural variations of thermal vias such as conformal vias vs fully-filled copper vias with various inside and outside via diameters, as well as copper thickness and pitch were also considered.

The structure is composed of multiple layers comprising of PA die, underfill, BGA, blind via, stack-up (polymer-glass-polymer), solder ball, copper pillar, PCB and a heatsink as shown in Fig. 2. The top most structure is a PA die: 3.5 mm x 2.5mm in dimensions and 0.1mm in thickness, which could be either CMOS or GaAs. Depending on the simulation scenario, an SOI is also considered above the hot-spot area with 1µm oxide thickness. The hot-spot is located on the bottom surface of PA die. A dissipation power of 0.7 W is imposed on the area, assuming a power efficiency of 30% for a 1 W chip. Six thermal micro-bumps and copper-filled blind vias are considered underneath the hotspot. The blind vias connect the copper pads between M1 and M2. In the stack-up, polymer dielectric is laminated on the top and bottom of the glass surfaces in order to buffer up the physical stress. TPV connects M2 to M3. Copper pillar connects the solder balls to the heat sink in PCB.

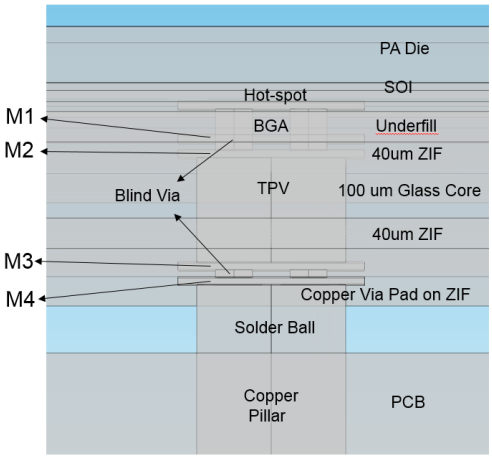

Fig. 2. Detailed structure for the modeling setup with COMSOL.

The following boundary conditions were applied for all the simulations.

- Heat Transfer Coefficient: $\underline{H = 10\ W/m^2K}$
- P_{Total} = 0.7 W was imposed on the Hot-spot; Heat flux = $\underline{0.7W / (0.25\ mm \times 0.35\ mm) = 8W/mm^2}$

Fig. 3 shows one example (six Blind Vias and a TPV) of the modeling with overall view, side view, and inner view of the structure. The diameter of blind via is 50µm, whereas the pitch

is 100µm. A single TPV has a diameter of 200µm. The geometry of the blind via and TPV was tailored for each simulation in order to study the effect of via geometry. Table 2 lists the materials and properties that were used in the COMSOL model construction.

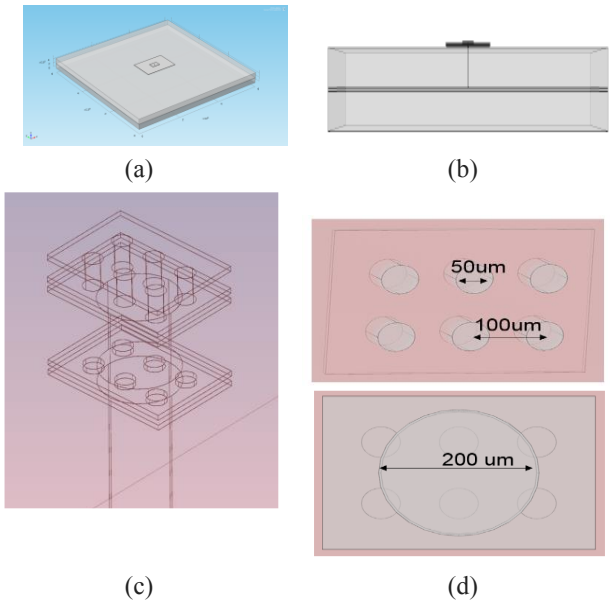

Fig. 3. COMSOL model construction: (a) Overall View, (b) Side View, (c) Inner View, (d) Diameter and pitch for Blind Via, and TPV.

Table 2. Materials and properties used for the simulation

	Heat Capacity [J/(kg·K)]	Density [kg/m^3]	Thermal Conductivity [W/(m·K)]
FR4	1369	1900	0.3
Silicon	700	2329	130
SOI	1000	2200	1.4
Underfill	800	1510	0.3
Polymer(ZIF)	936	2100	1
Glass	480	2200	1.1
Heat Sink	385	8700	400
Metal Pad	385	8700	400
Blind Via	385	8700	400
TPV	385	8700	400

Simulation Results

Four kinds of parameter were modeled: 1) Si vs. SOI, 2) location of die hotspot, 3) via geometry, and 4) conformal vs. fully-filled vias.

Si vs. SOI

With SOI wafers, transistors are formed in the thin layers of silicon that are isolated from the main body of the wafer by a layer of electrical insulator, usually silicon dioxide. Parameter 1 examines if SOI ICs affect the steady-state temperature on the hotspot area. Both the SOI and Si PA have the same number of Cu blind vias and a TPV, with hotspot location either at the center or at the corner. From Table 3, the SOI above the hot-spot blocked thermal conduction through the remaining PA die, resulting in a slight increase in the steady-state temperature.

Table 3. Simulation results for SOI vs. Si

	Model 1	Model 2	Model 3	Model 4
Hotspot Location	Center	Center	Corner	Corner
SOI	No	Yes	No	Yes
Steady-State Temperature	65.4°C	70.2°C	66.5°C	73.6°C

Location of Die Hotspot

Parameter 2 compares the thermal dissipation characteristics when hotspot is located at the center to that at the corner. Comparing Model 1 and Model 3 in Table 3, an insignificant difference in the steady-state temperature was observed, although the die was slightly cooler when the hotspot was at the center (Model 1). An example of simulation result with hotspot at the die corner is shown in Figure 4.

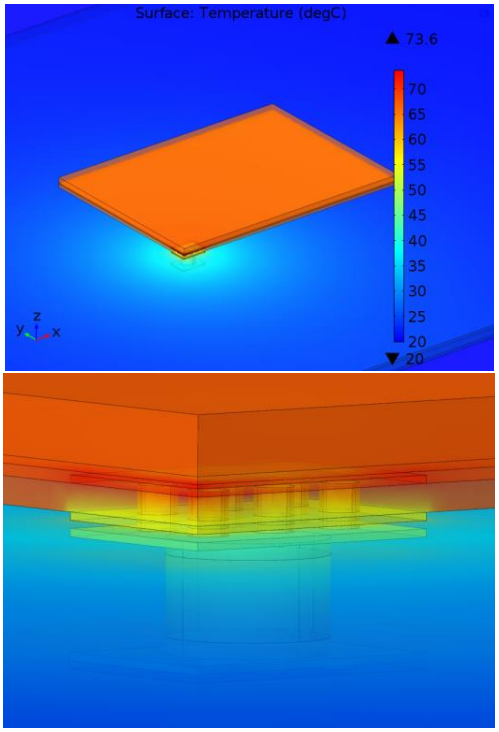

Fig. 4. An example of simulation result with hotspot at the die corner using an SOI PA die.

Via Geometry

Parameter 3 compares the steady-state temperature with the variations in via geometry. All simulations were conducted with fully-filled copper vias. The numbers of blind vias and TPVs were varied to investigate the cooling effect for each case. Model 1 in Table 4 shows that the most efficient way to cool the PA die is by using a direct TPV connection onto the die without any blind vias. Comparing Model 2 with Model 3, more blind vias with the same number of TPVs improved the heat dissipation from the hotspot. With the same number of blind vias, more TPV copper volume had better heat dissipation. When the total volumetric metallization between blind vias and TPVs is kept constant, the system achieved similar matched steady-state temperatures as seen in Table 4.

Table. 4. Simulation results with different via geometries

	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6
B.V. between M1 and M2	0	6	4	6	4	6
B.V. between M3 and M4	0	6	4	6	4	6
No. of TPV	1	1	1	2	2	4
Diameter/ Pitch (Blind Via)	NA	50µm/ 100µm	50µm/ 200µm	50µm/ 100µm	50µm/ 200µm	50µm/ 100µm
Diameter/ Pitch (TPV)	200µm/NA	200µm/NA	200µm/NA	100µm/ 150µm	100µm/ 150µm	100µm/ 150µm
Steady-state Temperature	52.9°C	65.4°C	86.1°C	76.7°C	90.1°C	65.9°C

Conformal vs. Fully-filled Vias

Parameter 4 inspects the impact of via type (conformal vs. fully-filled) and its thermal dissipation performance with variations in metal thickness. For the blind via BV, a diameter of 50µm is used, whereas 200µm is used for TPV's. Table 5 shows the trend of the steady-state temperature depending on the inside metallization thickness of via. The last row of the table illustrates that Model 1 shows the worst case of cooling scenario when both blind via and TPV have conformal metallization with 5µm metal thickness. In contrast, Model 5 demonstrates that when both blind and through vias are fully-filled, they could dissipate the heat most effectively. As the inside copper thickness increases, the steady-state temperature decreases accordingly, as seen from the transition between Model 1 and Model 5.

Table 5. Simulation results with different blind via and TPV combinations

	Model 1	Model 2	Model 3	Model 4	Model 5
Type of B.V.	Conformal	Fully-filled	Fully-filled	Fully-filled	Fully-filled
Type of TPV	Conformal	Conformal	Conformal	Conformal	Fully-filled
Inside Metallization Thickness (Blind via/ TPV)	(5µm/5µm)	(NA/5µm)	(NA/10µm)	(NA/15µm)	(NA)
Steady-state temperature	224°C	129°C	98.4°C	86.9°C	65.4°C

A proper combination of blind via and TPVs can be a very effective design feature for reducing the thermal resistance for multi-layer substrates, especially for glass packages. Thus, it is critical to choose the right via design, appropriate via count and efficient amount of copper metallization to optimize the package thermal design, while meeting the electrical constraints**.** The most efficient method to cool the PA die is to have a direct interconnection of TPV from the die to heatsink, which results in a steady-state temperature of 52.9°C. In such case, the fully-filled TPV with 200µm diameter would have substantial amount of copper inside, which requires new and innovative approaches for TPV filling. Even with a SOI PA and corner (unfavorable) hotspot locations, various combinations of blind vias and TPVs were able to achieve similar steady-state temperatures of 65.4°C and 65.9°C. Both of them satisfy the target steady-state temperatures of less than 85°C. A combination of via types, having 6 fully-filled blind vias and a single conformal TPV with 15µm thickness of metallization, resulted in a steady state temperature of 86.9°C, only slightly more than the target temperature at 85°C. Thus, further increase in the inside metallization (>15µm) would be able to meet the target steady-state temperature requirements at relatively low-cost because conformal vias take less time to electroplate.

Conclusions

An ultra-thin glass-based power amplifier module with copper through-vias was modeled for its thermal conduction characteristics. The impact of various design parameters was investigated through modeling to determine their efficacy in thermal management of power amplifier ICs. The location of hotspot was modeled as the first design parameter. The steady-state temperature did not vary significantly when the hotspot is either at the center or at the edge. The small difference came from the availability of more easily accessible surface area for heat spreading when the hotspot is at the die center. The second parametric study compared Si with SOI. In SOI, the oxide that isolates the Si from the device layer blocks the heat-transfer from the hotspot to the remaining part of PA die because of its poor thermal conductivity, resulting in a slight increase of the steady-state temperature. The models also quantitatively confirmed that the most efficient way to cool the PA die was to have a direct TPV with no blind vias since it provides the lowest thermal impedance. The steady-state temperature was lower with increasing number of blind vias or volumetric copper metallization. As the copper metallization inside the conformal via gets thicker, the steady-state temperature correspondingly decreases. The fully-filled copper vias provided the best option for PA cooling.

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