Nanowires-based High-density Capacitors and Thinfilm Power Sources in Ultrathin 3D Glass Modules

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Abstract:

This paper explores silicon nanowire technology for ultrathin high-density capacitors, supercapacitors and batteries. Development of such thin power components on glass or silicon will allow integration with other passive components as well as actives such as decoupling capacitors close to locic Ics to form 3D integrated passive and active devices (3D IPACs) that could then be surface-assembled onto glass packages leading to ultrathin self-powered modules or subsystems. Thinfilm integration of power components and passives on ultrathin glass 3D IPD substrates also leads to highly-efficient power distribution for miniaturized and high-performance electronic systems.

The first part of the paper presents an analytical model to highlight the benefits of nanowire electrode-based high-density capacitors in capacitance density and operating frequency. The second part of the paper describes nanowire synthesis and a novel fabrication process for nanowire-electrode capacitors, and their characterization. Results indicate that nanowires enable a major breakthrough in thinfilm capacitors with ultrahigh volumetric capacitance densities of about 100 μF /mm^3, 10X higher than all current capacitor technologies including trench, MLCC and tantalum capacitors.

I. INTRODUCTION

The primary drivers for electronic systems have been higher bandwidth and lower power, both enabled by the integration of ultra-thin active components in ultra-thin packages with higher interconnect density [1]. While major advances are being made in active devices and the interconnect densities with which to interconnect them with novel interposer and off-chip interconnection technologies, other system components for power storage, power conversion and power-supply with low impedance still remain as major fundamental bottlenecks. [2]. These components include batteries, storage components such as inductors and capacitors in VRM (voltage regulator modules) or DC-DC convertors, and decoupling capacitors.

Power components are discretely manufactured as individual components and surface-mounted on the board, far away from the active devices they serve. Their low volumetric densities and manufacturing limitations with today's microscale materials also results in thicker components. High-density passives such as Ta and Al capacitors are usually above 300 microns in thickness. MLCCs are being made thinner but are still discretely manufactured and assembled as SMDs. This leads to increased parasitics and reduced system performance. In the recent past, different methods to achieve high capacitance density and reduced component thickness have been explored. Etched Al foils help achieve the high capacitance densities in reduced component size, but suffer from lower volumetric density, frequency roll-off, reliability issues and integration challenges. Si trench capacitors have been explored, but have met limited success because of the very high costs. Integrating tantalum electrodes on silicon or glass creates process-compatibility challenges that still need to be solved. This paper explores silicon nanowires as an alternative electrode system to address these limitations. Silicon nanowires can achieve much higher volumetric density because of their nanoscale dimensions and much higher aspect ratio. Their process-compatibility with large glass panels also helps in substantially scaling down the cost. Silicon also forms a natural oxide with the highest electric field strength, which enables the thinnest dielectrics with the highest breakdown voltage. Hence, Si nanowires offer several advantages over the aforementioned technologies as they provide for higher densities, better reliability and manufacturability at lower-cost.

Silicon, in nanowire form, is a strategic nanomaterial for energy storage too. Silicon is an excellent host for lithium intercalation. By deposition of conformal thin lithium electrolytes and Li-Si anodes, high-energy density thinfilm batteries can be monolithically grown on glass substrates. The open structure of silicon nanowires allows easy expansion and contraction with lithium intercalation, thereby addressing the major fatigue concern with traditional silicon-based battery cathodes. Because of the low deposition temperature, nanowire batteries can be easily scaled and integrated using existing technologies, making them very attractive to both the silicon and packaging industry. Nanowires, therefore, offer unique benefits and can be used as novel building blocks for ultra-miniaturized passive components such as integrated passive devices (IPDs) with higher device integration [3,4,5,6,7].

Glass forms an ideal candidate for IPD substrate for thin components because of its ultra-thinness, low electrical loss, high resistivity, low-cost based ultrathin and large-panel processability. Recent innovations in through-glass vias will further improve the performance, reduce the final size and module cost. This paper advances the traditional IPD technology in two ways, 1.) Bringing heterogeneous component technologies to integrate batteries, storage capacitors and decoupling capacitors as double-side thinfilms that are compatible with through-vias,, as schematically

envisioned in Fig. 1a and 1b, 2.) Enhancing individual component characteristics, such as capacitance density using high aspect ratio nanowire electrodes. These 3D IPDs also enable double-side integration of actives and passives on an ultra-thin glass substrate to form a 3D Integrated Passive and Active Component (3D IPAC) module.

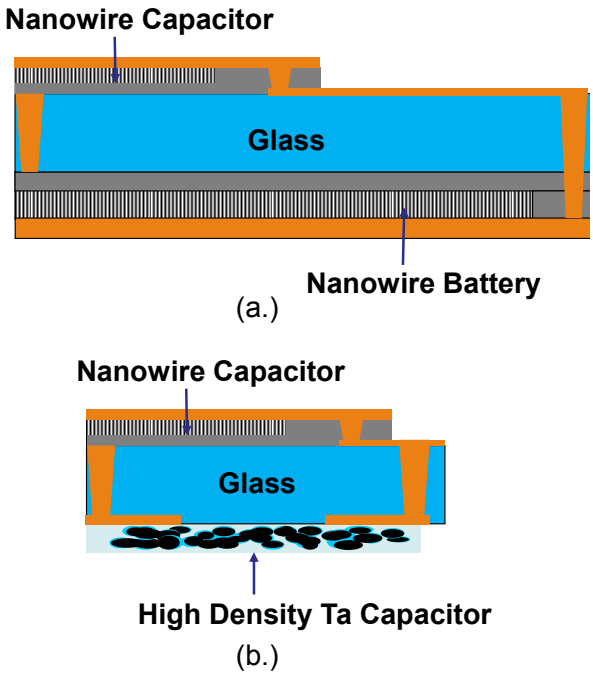

Fig. 1: Different configurations of Si-nanowire capacitors as 3D IPDs (a.) with Nanowire batteries to form self-sustained sub-system and (b.) with high density Ta capacitor to form a heterogeneous VRM+decoupling solution.

This paper primarily focuses on exploring and demonstrating silicon nanowires for power components, using capacitor as an example, which can be then extended to batteries and other storage components such as supercapacitors. The paper is organized as follows: Section II presents an analytical model to determine the voltage levels required to achieve maximum capacitance based on intrinsic doping concentration in silicon. Section III describes the fabrication process for the Si nanowire capacitor. Section IV presents the characterization and Section V summarizes the key findings.

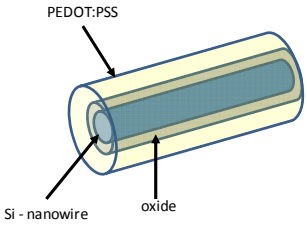

Fig. 2: Schematic representation of an individual nanowire capacitor.

II. Analytical Model

Silicon nanowire capacitors are essentially metal-oxide-semiconductor type capacitors. Fig. 2 shows a simple schematic of the structure. The capacitance of a MOS structure depends on the voltage bias applied to the metal (gate). The capacitor can operate in three different states based on the voltage applied, as is seen in Fig. 3. The states can be classified as (i) Accumulation: Surface accumulation of carriers that are same as the majority carriers in the bulk, (ii) Depletion: No carriers present on the surface with only a space charge or depletion region is present and (iii) Inversion: Opposite charge carriers to those present on the body accumulate on the surface. Two voltages can be used to effectively separate these three different regions. These are (a) Flatband Voltage: It helps separate the accumulation region from the depletion region and (b) Threshold voltage: Helps separate the depletion region from the inversion region. This paper focuses only on the accumulation region for a MOS capacitor. Based on the calculated capacitance and resistance, the RC time constant for such capacitors can be estimated.

1. Nanowire Length approximation:

When Au is used as a catalyst, the nanowire length can be estimated using Equation 1, where L is the length of the nanowire, r is the radius at the base, a^3 is the atomic volume of Au and theta is the average Au coverage on the sidewalls. Theta has been estimated to be 1 – 1.5 monolayers [8]. Table 1 summarizes the approximate length of nanowires that can be grown based of the Au catalyst size.

$$L = \frac{r^2}{2a\theta} \qquad (1)$$

2. Nanowire Resistance:

Given a certain conductivity of the silicon, the resistance of the nanowires can be estimated. The following equations allow to calculate the resistance based on the doping concentration.

$$R = \frac{\Delta l}{\sigma S} \qquad (2)$$

Where R is the resistance in ohms, Δl is the length of the nanowire in meters, σ is the conductivity in Siemens/m and S is the cross-sectional area of the nanowire. The conductivity of an intrinsic semiconductor is defined as

$$\sigma = n_i(\mu_e + \mu_h)q \qquad (3)$$

where n_i is the intrinsic carrier concentration, q is the charge of the electron ($1.6\text{x}10^{-19}$ C), and μ_e and μ_h are the mobilities of the electrons and holes respectively. For an extrinsically doped semiconductor, either the electron or hole concentration will dominate and hence the other can be ignored while calculating the conductivity. It is well known that for an intrinsic semiconductor there is no net charge. This remains same even for extrinsically doped semiconductors. This means that even after doping, the total number of positive charges equals the total number of negative charges. This is derived from the Mass-Action law, which states that

$$np = {n_i}^2 \quad (4)$$

For extrinsically doped n-type semiconductor:

$$\sigma = n\mu_e q \quad (5)$$

For extrinsically doped p-type semiconductor:

$$\sigma = n\mu_h q \quad (6)$$

where n in the above equations can be replaced with N_D or N_A based on the doping type.

Table 1: Analytical modeling data showing capacitance and cut-off frequency as a function of Au catalyst size

Si – type	Au catalyst size (nm)	Length of wire (m)	Resistance (Mohms)	Capacitance (fF)	RC time constant (nS)	Cut-off frequency (MHz)
5 ohm-cm	30	1.731	30	2.2	66	2.4e6
	50	4.8	31	9.4	$0.3x10^3$	0.53
	100	19.23	31	70	$2.1x10^3$	$75.7x10^{-3}$
10 ohm-cm	30	1.731	60	2.2	132	1.2
	50	4.8	62	9.4	$0.6x10^3$	0.26
	100	19.23	62	70	$4.2x10^3$	$37.5x10^{-3}$

The volumetric capacitance density was calculated based on the capacitance from Table 1. The total number of nanowires per unit area was estimated based on the nanowire diameter and minimum distance between two wires. The density was estimated to be 100 – 150 μF/mm^3. This value is 10X higher than current capacitor technologies, and 2X higher than what is projected as the maximum achievable density with existing capacitor technologies.

3. Flatband voltage and Cut-off frequency:

This phenomenon takes place when the voltage applied is greater than the flatband voltage (positive or negative depends on substrate type). The flatband voltage is the voltage at which no charge is present on the capacitor electrodes leading to no electric field across electrodes. The flatband voltage depends on the doping concentration of Si. It is also highly dependent on any residual charge that may be present at the interfaces and across the electrodes. Hence, when a voltage greater than the flatband (large negative voltage for a p-type substrate) voltage is applied, it causes the holes to be attracted to the interface causing accumulation. The opposite is true for an n-type substrate [9]

$$V_{FB} = \phi_m - \phi_s \quad (7)$$

$$\phi_s = \chi - \frac{E_g}{2q} - V_t Ln\left(\frac{N_a}{n_i}\right) \quad (8)$$

$$\phi_s = \chi - \frac{E_g}{2q} + V_t Ln\left(\frac{N_d}{n_i}\right) \quad (9)$$

$$V_t = \frac{KT}{q} \quad (10)$$

A p-type substrate is considered in this analysis; hence the threshold voltage is defined as

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s N_a \phi_F}}{C_{ox}} \quad (11)$$

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r A}{d} \quad (12)$$

where Φ_m is the work-function of the metal gate, Φ_s is the work-function of Si, χ is the electron affinity, Φ_F is the bulk potential of Si, ε_s is the relative permittivity of Si, C_{ox} is the oxide capacitance (under accumulation), K is the Boltzmann's constant, T is the temperature in K and q is the charge of an electron in C. It is important to calculate the threshold voltage and the flatband voltage, as this will allow capacitor operation in accumulation, resulting in maximum capacitance [10, 11].

Based on the above equations, the capacitance and resistance is calculated and the RC time constant can be estimated as

$$\tau = RC \quad (13)$$

And the cut-off frequency is estimated as

$$\tau = \frac{1}{2\pi f_c} \quad (14)$$

$$f_c = \frac{1}{2\pi\tau} \quad (15)$$

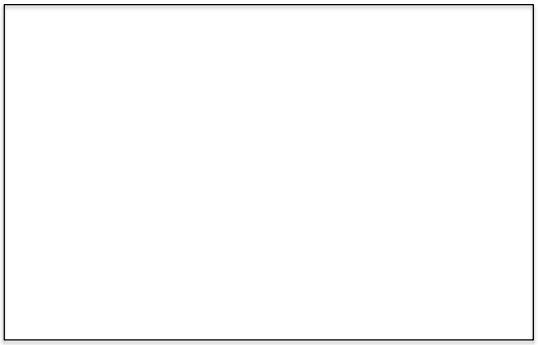

Fig. 3: Representative MOS capacitance. Graph shows voltage-dependent capacitance.

Table 2: Analytical flatband and threshold voltages

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	Copper	N^+ Poly	P^+ Poly
V_{FB} (V)	-0.36	-0.87	0.23
V_T (V)	0.37	-0.14	0.96

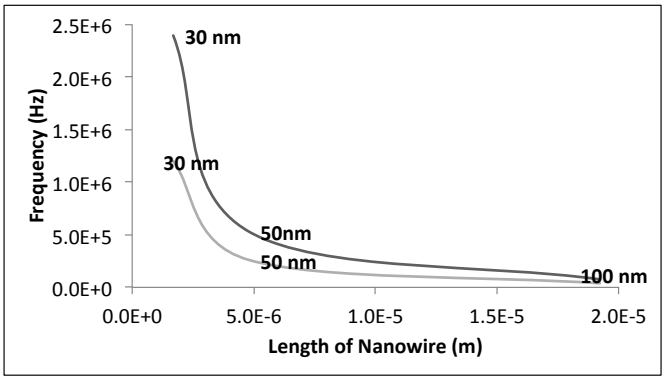

Fig. 4: Change in cut-off frequency with increasing nanowire length. It is important to note that the length of the nanowire changes based on the size of the Au catalyst.

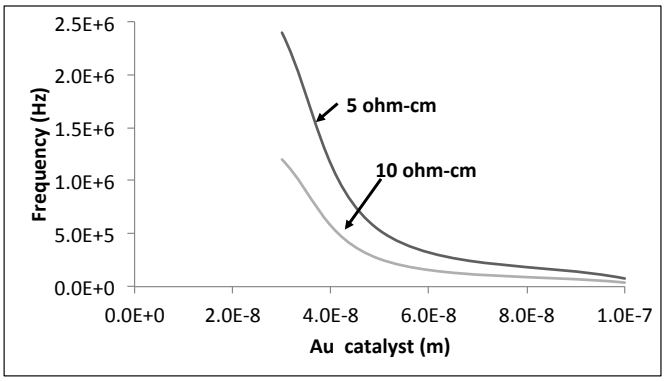

Fig. 5: Change in cut-off frequency with respect to Au catalyst size.

Cut-off frequency, the frequency above which the capacitor performance degrades, is an important factor in power supply design. Using Equations (13-15), Fig. 4 and Fig. 5 show the cut-off frequency with changing wire length and catalyst size respectively. The cut-off frequency is inversely proportional to increasing R and C. Hence, with increasing wire length, both resistance and capacitance increase but cut-off frequency decreases.

III. Fabrication

Capacitors were fabricated with Si-nanowires as the bottom electrode, thin-oxide as the dielectric and PEDOT:PSS (poly(4,5 ethylene dioxy thiophene) – poly(styrene sulphonate)) as the top electrode. The nanowires were fabricated using two different techniques: 1. CVD growth and 2. Etching. The oxide was formed using a novel thermal oxidation technique and finally the top electrode was formed dispensing PEDOT:PSS nanosuspension. Next, each of the steps in the fabrication process is explained in detail. A schematic of the entire fabrication process is seen in Fig. 6.

1. Nanowire Fabrication:

The bottom electrode of the capacitor was formed by the nanowires. Nanowire fabrication was carried out using two different methods.

a. CVD Growth:

The experiments to grow Si nanowires were carried out using a CVD furnace. The nanowires were grown on a Si(111) substrate. The substrate was cleaned to remove any natural oxide using 10% hydrofluoric acid. Gold catalyst was then deposited using a colloidal gold suspension. This allows for the Au to be distributed on the substrate. Gold particles with various diameters were used as the gold catalyst. It was seen that the 50 nm particles consistently produced nanowires. The substrate with gold catalyst was placed in the CVD chamber. The temperature was maintained between 410 – 430 ^{o}C. A mixture of silane gas (15%) and hydrogen gas (85%) (carrier) was used. The process was run for 10 minutes. The nanowires grown from these experiments are completely random in orientation. More control over the process parameters can yield extremely directional wires. For capacitors, the random orientation of the wires can be an advantage as it provides considerably more surface area than vertical wires and increases the overall capacitance density. Hence, there was no further effort to improve the orientation of the nanowires.

b. Etching:

An alternative approach based on etching process was also utilized to form the Si nanowires. The etching process uses Au as the catalyst, which is then patterned into nanoscale islands using e-beam nanolithography. It was seen that the gold was more stable compared to colloidal gold catalyst used for the CVD process. It did not move and diffuse into other gold droplets. The etching solutions consisted of a mixture of hydrofluoric acid and hydrogen peroxide. The Si was etched only in locations were Au catalyst was present, leaving the Si around it unaffected. This allowed for extremely vertical Si nanowires. This process requires more control than the CVD process as any change in the etching mixture could result in unwanted etching and pit formation on the Si surface. This is highly undesirable when trying to achieve high aspect ratio structures.

2. Oxidation:

The next step in the capacitor fabrication process after nanowire fabrication is the formation of the dielectric. Silicon oxide has the highest electric breakdown strength because of its large bandgap, making it withstand sufficient voltages even when thinned down to 10s of nm. It is also important to note that the deposition of high-k dielectrics such as barium strontium titanate in high-aspect ratio structures such as these nanowires would be extremely challenging. Hence, silicon oxide was the dielectric of choice for these capacitors using a novel technique for low-temperature (<500 C) oxidation.

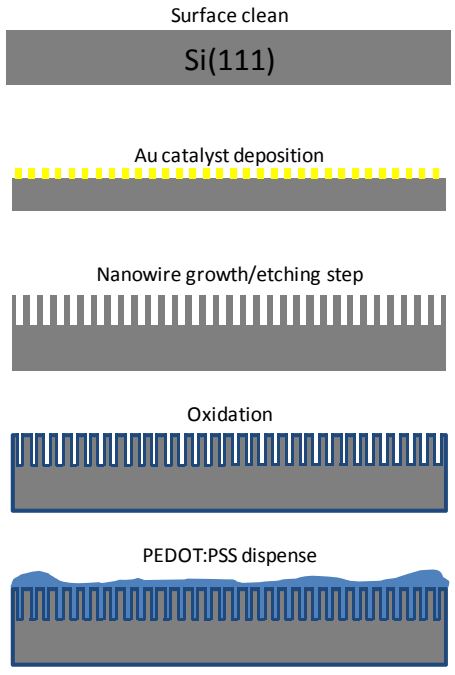

Fig. 6: Fabrication process for capacitor formation starting from surface preparation to top-electrode formation.

3. Top Electrode using PEDOT:PSS

Conducting polymer (PEDOT:PSS – poly(4,5 ethylene dioxy thiophene) – poly(styrene sulphonate)) was used as the cathode for the silicon-nanowire systems. PEDOT:PSS is the most widely used conducting polymer in the capacitor industry. PEDOT:PSS has a high conductivity (~600 S/cm), which results in extremely low ESR compared to other cathodes such as MnO2 and is self-healing in nature. Self-healing in PEDOT:PSS leads to burning of the cathode next to a defect site in dielectric, thus, preventing a short between the cathode and the anode. This also helps in minimizing the leakage current.

IV. Characterization

The morphology of the nanowires was studied using scanning electron microscopy (SEM). The oxide was studied using SEM and X-ray photon spectroscopy (XPS). The capacitor was tested using a liquid electrolyte as the cathode. Each step is briefly discussed below.

a. Morphology of Si-Nanowires

The Si-nanowire samples were characterized using scanning electron microscopy (SEM) to study the morphology. It was seen that nanowires that were grown using the VLS (Vapor-Liquid-Solid) technique in the CVD chamber were randomly oriented. This is desirable as the resultant porous structure allows for extremely high surface area that can lead to very high capacitance density. SEM image of the randomly-oriented nanowires is shown in Fig. 7. The length of the nanowires was measured to be around 3 – 3.5 micron, with a Au catalyst size of 50 nm. The analytical modeling shows that the length should be around 5 micron. The limited growth is attributed to the small processing times used (< 10 minutes). Nanowires formed using the etching processes were also characterized, as shown in Fig. 8. It was seen that the wires in this case were completely vertical. The length of all the wires was almost the same, indicating minimal standard deviation. In case of the etching process, the length of the wires was highly dependent on the etching times.

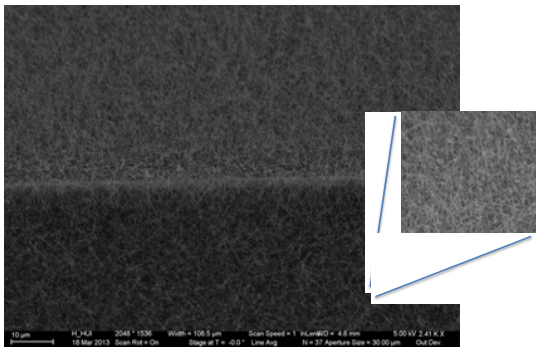

Fig 7. Morphology of Si-nanowires using FE-SEM. Image shows randomly orientated nanowires grown using CVD.

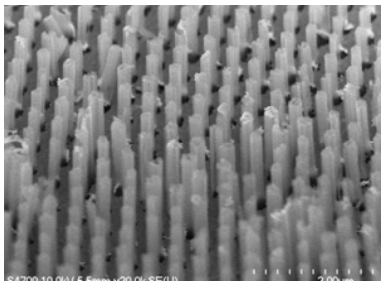

Fig 8. Morphology of Si-nanowires using FE-SEM. Image shows extremely vertical nanowires formed using an etching process.

b. Capacitor Characterization:

The fabricated devices were characterized for capacitance and leakage currents. For measuring the ideal capacitance density of the device utilizing all the electrode area, liquid electrolyte testing with a set-up shown in Fig. 9 was used. The silicon nanowire capacitor was used as the anode whereas sulfuric acid with a concentration of 0.5 M was used as the electrolyte, in addition to working as a cathode. The presence of an electrolyte leads to additional capacitance due to the formation of the electrochemical double layer at the oxide-electrolyte interface. A schematic of the interfaces involved in the capacitor system is presented in Fig. 9 to illustrate the capacitance contribution from the silicon oxide and the electrochemical double layer. As seen from the figure, the capacitance contribution from the double layer and the oxide are in series. With such series capacitors, the smaller capacitor dominates the capacitance. The net capacitance for this capacitor series is therefore determined by the contribution from the nanowire because the double-layer capacitance is much higher. The capacitance is calculated as:

$$C = \frac{A\varepsilon\varepsilon_r}{t} \tag{16}$$

where A = Surface area of the electrode, ε = Permittivity in vacuum, ε_r = Relative permittivity of the dielectric, and t = thickness of the dielectric.

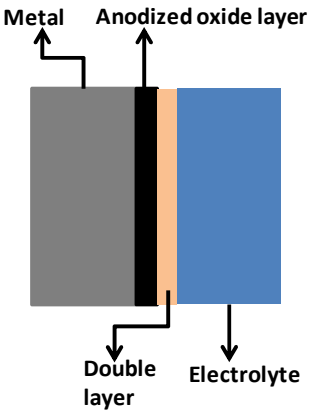

Fig. 9 Interface involving two dielectrics in the wet-system *(metal oxide and electrochemical double layer)* [12].

Assuming the surface area (A) of the double-layer and oxide capacitors to be the same, ε_{r1} and t_1 = permittivity and thickness of the oxide layer, ε_{r2} and t_2= permittivity and thickness of the double layer, C1 = capacitance from the oxide layer, C2 = capacitance from the double layer;

$$\varepsilon_{r1} << \varepsilon_{r2}; \quad t_2 << t_1 \Rightarrow C_1 << C_2$$

Here, since C1 and C2 are in series,

$$C_{eff} = \frac{(C_1 \times C_2)}{(C_1 + C_2)} \cong C_1 \qquad (17)$$

Hence, the capacitance measurement obtained using this set-up can be approximated as the capacitance from the silicon nanowire electrode. Capacitors with solid cathodes based on PEDOT-PSS were characterized by directly probing the cathode and anode surfaces.

The measurement results showed a maximum capacitance density of 20 μF/cm^2 with liquid-electrolyte testing. A leakage current of 1 μA/μF was recorded. When compared to planar silicon oxide capacitors with 50 nm oxide films, this approximates to a 40 X enhancement in surface area in spite of being only 2 microns thin. The nanowire electrodes result in a high volumetric density compared to other thin capacitor approaches. As seen in Fig. s 4 and 5, it is estimated that the capacitors will be limited in frequency performance to lower kHz. This is attributed to the extremely high resistance of the nanowires with test silicon wafers (1-10 ohm cm resistivity). With low-resistivity doped silicon, the conductivity can be further enhanced to improve the operation frequency of these capacitors.

Compared to alternative substrate-compatible high surface area electrode techniques such as trench capacitors or nanoparticle electrodes, the etched nanoelectrode process is much simpler and allows easy scale-up at low cost. The results therefore represent a significant breakthrough and advance in nanocapacitor technologies.

V. Summary

A novel process to achieve ultrahigh-density capacitors was demonstrated using Si nanowire electrodes. An analytical model was developed to predict the length of the nanowire, the capacitance density and frequency-stability that can be achieved. The flatband voltage and the threshold voltage were also calculated. This helps to determine the required voltage for the MOS device to operate in accumulation mode for maximum capacitance density.

Nanowires were formed using two distinct processes: 1). VLS growth technique using CVD and 2) Wet-etching process. SEM was used to characterize the wires. The VLS growth technique produced randomly-oriented wires that are desirable as they enable very high capacitance densities. The etching process, on the other hand, provided vertical nanowires. Thin oxides were grown using a novel thermal oxidation process. Finally, top electrodes were formed using PEDOT:PSS (conducting polymer). A capacitance density of 20 μF/cm^2 was measured for a 2-micron film, indicating a volumetric capacitance density of 100 μF /mm^3, 10X higher than other current capacitor technologies. The new, nanowire-based approach can also be extended to supercapacitors and batteries to enable completely self-powered modules.

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