Modeling, Fabrication, and Characterization of Low-Cost and High-Performance Polycrystalline Panel-Based Silicon Interposer With Through Vias and Redistribution Layers

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Abstract—Interconnections between integrated circuits and print circuit boards are primarily achieved currently with organic packages at high I/O pitch. Organic packages, however, are limited by poor thermal and dimension stabilities for them to act as fine pitch interposers. To address these challenges, silicon interposers are being developed. Current silicon interposers, based on through-silicon via (TSV) techniques, suffer from high production cost, because of expensive CMOS-grade silicon, expensive TSV process and smaller wafer sizes. They also suffer from high electrical loss in spite of thin SiO2 interfacial layers. This paper, for the first time, demonstrates a lower cost and higher performance silicon interposer. It is based on panel-based polycrystalline silicon with through-package vias (TPVs) and redistribution layers, and a simple and double-side process with thick polymer liner inside the TPV. Electrical modeling was carried out that shows the better electrical performance of polycrystalline silicon interposer compared with traditional single-crystalline silicon interposer. The polycrystalline silicon interposer test vehicles with up to four metal layers were demonstrated and characterized. The measurement results showed good electrical performance and matched well with the simulations.

Index Terms—Double-side process, insertion loss characterization, polycrystalline silicon panel, silicon interposer.

I. INTRODUCTION

INTERPOSERS by definition connect two or more integrated circuits (ICs) with fine pitch I/Os, typically at or below 40-μm pitch on the top side and at larger pitch with flip-chip assembly on the bottom side [1]–[4]. Organic substrates have not been developed into these fine pitch interposers due to their limitations in dimensional and thermal stabilities [5]. Interposers to date have been silicon interposers only, with through-silicon-vias (TSVs) processed in single-crystalline silicon wafers. The requirement for through-via densities strongly depends on the applications. For example, high via densities are necessary for applications like 3-D ICs. While applications, such as 3-D wafer-level-packaging or microelectromechanical systems packaging, require significantly lower via densities [6], [7]. The silicon interposer in this paper intends to provide a low-cost solution for the latter applications and yet achieve high performance.

The fabrication of traditional silicon interposers with TSV usually involves the well-known Bosch process [8], [9] to form blind vias in single-crystalline silicon wafers. Inside these TSVs, thin layers of SiO2 are widely used as the liners to insulate the lossy silicon. There is also the need for diffusion control between copper inside TSV and silicon, which is typically accomplished using barriers such as Ti, TiN, and TaN [10], [11]. The Cu seed is then formed using sputtering process and the via is then filled with Cu by electroplating. A chemical mechanical polishing (CMP) process is necessary to expose the Cu via. Although silicon interposers have been developed to address I/O pitch limitations of organic interposers, they have their own challenges. Since the number of interposers coming from 200- to 300-mm silicon wafers is low, particularly if the interposers are 50–60 mm in size, serious cost concerns remain as the biggest barriers to adoption of silicon interposers. Additional challenge with silicon interposers is to do with electrical loss of silicon in spite of SiO2 dielectric layer. This is always recognized as the second major concern with traditional silicon interposers. Tezcan et al. [12] developed a polymer-lined TSV involving etching an annular hole in silicon, filling it with polymer, and finally etching out the silicon core. Such a process, however, increases the number of steps to the already complex and expensive process to form silicon interposers.

This paper addresses both the shortcomings of traditional silicon interposers by presenting an entirely different approach using polycrystalline silicon in large panel form and thick insulating polymer liners. Polycrystalline silicon in panel form is widely used in photovoltaic industry and has been extensively studied as a substrate for solar applications [13]–[15]. However, it has never been studied as the electronic substrate material for the interposer applications. Polycrystalline silicon,
as an interposer substrate, has a few advantages; simpler to fabricate than single-crystalline silicon and can be scaled to large panel sizes up to 700 mm. This large size will lower the cost of interposers by yielding more interposers. In this paper, small 150 mm \( \times \) 150 mm polycrystalline silicon panels (shown in Fig. 1) with thickness of 200 \( \mu \)m are used. These panels are fabricated using directional solidification technique, which forces the impurities to segregate into melt [16]. Due to its lower purity levels, polycrystalline silicon material presents a much lower resistivity than the traditional single-crystalline silicon. The issue is proposed to be addressed by a low-cost and thick insulating polymer liner on the walls of through vias. Table I summarizes a comparison between the polycrystalline silicon interposer and traditional single-crystalline silicon interposer.

A cross section schematic of the polycrystalline silicon interposer with through-package-vias (TPVs) and assembly of multiple ICs is shown in Fig. 2. The double-side approach used in integrating the components on both sides will result in a reduced interposer size, leading to a miniaturized package with even lower cost.

This paper presents a first, pioneering research to explore polycrystalline silicon in large panel form as a low-cost and high-performance interposer. It presents a combination of materials and processes to form TPVs and redistribution layers (RDLs). This paper has four sections. Sections I and II present the electrical modeling results, showing the performance comparison between TPVs in polycrystalline silicon interposers and TSVs in traditional silicon interposers. The detailed double-side fabrication process is presented in Section III. Section IV summarizes the fabrication and electrical characterization of polycrystalline silicon interposer with up to four-metal RDL structures, including insertion loss in coplanar waveguide (CPW) lines and TPV structures. Finally, the conclusion is drawn in Section V.

### II. Electrical Modeling of TPV in Polycrystalline Silicon Interposer

In this section, the electrical performance of polycrystalline silicon with TPV is simulated and compared to single-crystalline silicon with TSV. The 3-D electromagnetic software High Frequency Structural Simulator was used to simulate the through-via structure, as shown in Fig. 3. The structure consists of two signal vias (marked as S) and four ground vias (marked as G).

![Fig. 2. Cross section schematic of polycrystalline silicon interposer with TPVs, wires and different ICs on both sides.](image2)

![Fig. 3. Schematic of (a) top view and (b) cross-sectional view of the Ground-Signal-Ground model.](image3)
A typical 10 Ω-cm silicon material with 1-μm SiO₂ liner was used as an example for single-crystalline silicon interposer; while a much lower, 0.5 Ω-cm silicon, with a 3-μm thick, low loss polymer liner (tan δ = 0.002) was used in the polycrystalline silicon interposer. The via diameter, via pitch and silicon thickness were all the same for two different cases. Both silicon interposers were 200 μm in thickness. The diameter and pitch of these Cu-filled vias were 30 and 60 μm, respectively. Fig. 4 compares the insertion loss and far-end crosstalk (FEXT) between the two different silicon interposers. The TPV in polycrystalline silicon interposer shows a lower insertion loss and crosstalk up to 10 GHz. The superior electrical performance of such interposer is due to the thick polymer liner on both surfaces and via side-wall. This helps reduce the substrate loss and coupling in the silicon substrate.

Parametric studies of electrical performance on TPV in polycrystalline silicon interposer were also carried out. Both the effects of in-via polymer liner thickness and TPV diameter have been simulated. Detailed geometry and material information can be found in [17]. These results show that the insertion loss and crosstalk can be reduced using a thicker sidewall liner. On the other hand, the electrical performance in the TPVs can also be improved by decreasing the via diameter since smaller TPVs have smaller sidewall capacitance (due to smaller diameter) and smaller substrate conductance (due to larger spacing between the TPVs). This helps in reducing the loss and their crosstalk is lower compared with the larger TPVs because of the greater spacing between the smaller TPVs.

The effects of the thickness of surface liner (3, 20, and 40 μm) on insertion loss and FEXT were also simulated and the results for up to 10 GHz are summarized in Fig. 5. The silicon substrate was 200 μm in thickness with a resistivity of 0.5 Ω-cm. The vias had a diameter of 30 μm with a pitch of 60 μm. The in-via liner was 3-μm thick. Fig. 5 shows that a thicker surface liner can result in lower insertion loss and FEXT.

III. PROCESS FLOW

The process flow used to fabricate polycrystalline silicon interposer, with up to four metal layers, is summarized in Fig. 6. It consists of four steps: 1) TPV formation; 2) TPV liner formation; 3) TPV metallization; and 4) RDL fabrication. Compared to the published TSV processes, the approach used in this paper includes:

1) unique double-side TPV process, including:
   a) laser ablation for via formation;
   b) thick polymer liner fabrication;
   c) dry film lithography, electro-less plated seed, and through-via filling, without any CMP process;
2) double-side process for RDLs.
1. **TPV Formation**

![Diagram of TPV Formation]

![Diagram showing process flow for fabricating polycrystalline silicon interposers with TPVs and RDLs.]

2. **TPV Liner Formation**

![Diagram of TPV Liner Formation]

3. **TPV Metallization**

![Diagram of TPV Metallization]

4. **RDL Fabrication**

![Diagram of RDL Fabrication]

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### A. TPV Formation

Laser ablation is a feasible technique to form vias in polycrystalline substrates and it can be scaled to large panels [18]. Three different laser technologies (UV, excimer, and picosecond laser) were explored for via formation. All the through-vias were formed in the 200-μm-thick polycrystalline silicon panels as shown in Table II, which compares the output differences among the three laser technologies.

Both small and large vias were formed by UV laser, operating at 355 nm. The ArF-based excimer laser processing with a wavelength of 193 nm was found to be more effective, resulting in less thermal damages. Smaller vias without any taper were achieved in 200-μm-thick polycrystalline silicon substrate with excimer laser technique. But, this technology suffers from high production cost. The 355-nm picosecond lasers can further reduce the heat generated during the laser ablation process. Vias from 10- to 50-μm diameters were formed by picosecond lasers. However, this method is currently limited by slow processing speed.

Considering both the throughput and cost, UV laser, operating at a wavelength of 355 nm, was chosen for TPV formation with vias of 80-μm diameter. The top view of the laser drilled vias is shown in Fig. 7.

### B. TPV Liner Formation

The technical approach for the liner formation involves polymer filling in TPVs, followed by laser ablation to form an inner via, leading to in-via thick polymer liners with controlled thickness. The polymer liner serves to replace both the SiO₂ and diffusion barrier in traditional TSVs.

The laser drilled silicon samples were first cleaned using plasma treatment. The silicon surface was treated with silane solution (3-aminopropyltrimethoxy silane), which leads to the formation of covalent bonds at the interface between silicon and polymer to improve adhesion. The polymer film was laminated to fill the TPVs. The lamination process can also form polymer layers on top and bottom sides of the silicon panel for insulation purposes. Two methods, with roll lamination and vacuum lamination, were used and evaluated for polymer filling. Fig. 8 shows a comparison between the single-side and double-side lamination processes.

The single-side roll lamination process was first studied. However, voids were observed between polymers after filling. These voids create potential problems for the following laser ablation step. The new polymer filling method using vacuum laminator was then carried out. Both sides of the silicon substrate were laminated at the same time, leading to a faster, void-free filling process for the 200-μm-thick silicon substrate with through vias of 80-μm diameter. Adhesion between
polymer and silicon was measured qualitatively by tape test for peel strength and the samples showed good adhesion.

The inner vias with a diameter of 40 μm were then fabricated by UV laser ablation as shown in Fig. 6, resulting in a 20-μm-thick polymer liner. The thickness of the polymer on substrate surfaces was 40 μm.

C. TPV Metallization

The metallization process consists of three steps: 1) Cu seed layer formation; 2) Cu electroplating; and 3) pad formation. The polycrystalline silicon sample with polymer liner was first cleaned using plasma to remove any impurities on the surface. A low cost, double-side electroless plating process (20 min) then was used to fabricate a 1-μm-thick Cu seed layer. A void-free double-side Cu electroplating was performed in the plating tank to fill the through vias. A current density of 4 A/cm² was used in this process for 2 h. The Cu overburdens on the surfaces were thinned down to 12 μm by a double-side chemical etching process. Dry film polymers were laminated on both surfaces of the sample followed by a lithography process to pattern the traces. The Cu was then etched by dilute CuCl₂ solution and photoresist was stripped by potassium hydroxide to finally form the Cu pads.

D. RDL Fabrication

To fabricate the RDLs, another two build-up polymer dielectric layers were formed on the surface by double-side vacuum lamination processes. Then, 355-nm UV laser ablation was used to form blind microvias in the cured polymer. The microvias and build-up layers were covered by 1-μm-thick Cu seed layer with electroless plating, followed by semiadditive plating with double-side dry film photoresist lamination and lithography process. The final steps included the Cu seed etching by CuCl₂ solution and photoresist stripping.

IV. Test Vehicle Fabrication and Characterization

By integrating the processes presented in Section III, the polycrystalline silicon interposer test vehicles were successfully fabricated. Fig. 9 shows the top view of the completed 150-mm × 150-mm size polycrystalline silicon panel with TPVs and RDLs on both sides. The mask design involves transmission lines with different lengths as well as CPW-TPV transitions. The microsection photograph of the four-metal layer interposer is shown in Fig. 10.

The insertion loss of CPW traces was measured and the results were compared with the simulation results for correlation. 160-μm wide transmission lines with a gap of 36.5 μm between the signal and ground were fabricated. The vector network analyzer measurements were performed up to 10 GHz, after calibrations. Fig. 11 shows the simulation and insertion loss measurements for both 6.2- and 11.2-mm CPW traces without vias. Fig. 11 shows that the 6.2- and 11.2-mm transmission lines had <1.5 and 2.5 dB insertion loss, respectively at 10 GHz. This translates to a loss of 0.24 and 0.22 dB/mm at 10 GHz, respectively. The low insertion loss in CPW trace matched the simulation results very well. However, longer traces followed the trend of increased insertion loss rapidly. This decreased the overall signal quality.

The insertion loss of CPW-TPV transition in the two-metal layer structure is shown in Fig. 12 with signal lines of different lengths. The impact of transmission line length on the insertion loss was studied. The results show that the insertion loss increased with larger signal length but the total impact of length increase on the insertion loss at lower frequencies was negligible. Thus, local routing can be performed in the
interposer between signal TPVs without significant impact on the signal quality. The model-to-measurement correlation was also conducted and a good model to hardware correlation was observed.

Electrical performance of CPW lines and via transitions in structures with up to four-metal layers was also characterized and insertion loss results were compared in Fig. 13. The length of the CPW line was fixed at 1 mm. As shown in Fig. 13, the one-metal layer structure consisted of only the transmission line on the top metal layer, while the two-metal layer structure included blind vias, which can transfer signals to the second metal layer. Both the three-metal layer and four-metal layer structures included TPVs to connect the lines to the metal layers on bottom side. These measurements show that the insertion loss increased with the frequency. The loss also increased with the number of metal layers. This is due to the added loss, coming from via transitions. The overall loss was low and remained below 0.9 dB at 2.4 GHz for the four-metal layer structure. This result indicates that multiple signal layer escape routing is possible due to the good isolation of the thick polymers to achieve low loss silicon interposers.

V. Conclusion

This paper presents, for the first time, the modeling, fabrication, and characterization of polycrystalline panel-based silicon interposer as a low-cost and high-performance solution for packaging next generation ICs. These interposers were fabricated with lower cost, and lower resistivity polycrystalline silicon, compared with higher cost and higher resistivity single-crystalline silicon. Through via formation in these interposers was achieved using 355-nm UV laser. Thick polymer liner, that is, proposed to reduce the silicon loss, was formed with a low cost, double-side process. The polycrystalline silicon interposer test vehicle with metallized TPVs and RDLs were successfully demonstrated. Both electrical modeling and characterization results indicate that polycrystalline silicon interposer can achieve high performance.

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References


