High-Frequency Characterization of Through Package Vias Formed by Focused Electrical-Discharge in Thin Glass Interposers

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Abstract

This paper presents the modeling, design, fabrication and characterization, up to 30 GHz, of low loss and high aspect-ratio 55 μm diameter through package vias (TPVs) in 300 μm thick glass interposers. These TPVs were fabricated using a novel, high-throughput, focused electrical discharge method and low cost panel-based double-side metallization processes. Such a glass interposer is targeted at two emerging applications, (a) large 30 mm to 60 mm body size 2.5D interposers to achieve 28.8 Gbps logic-memory bandwidth and (b) 3D interposers for mm wave applications at 28 GHz local multipoint distribution service (LMDS) for future 5G networks. Accurate measurement of the electrical performance of fine pitch metallized through vias in glass up to 30 GHz and beyond is critical for both these high performance interposer applications. In this paper, two novel characterization methods are applied: 1) the short-circuit-and-open-circuit method and 2) the dual-via-chain method. The resistance and the inductance of a single via are extracted by using a short-circuit structure along with an open-circuit structure. At 10 GHz, the values for the series resistance and inductance have average values of 0.1 Ω and 160 pH respectively. Long dual-via chains were designed to evaluate their performance in insertion loss, delay and eye diagram. The insertion loss achieved with the longest dual-via chain was found to be less than 1 dB/cm up to 30 GHz with only a 6.2 ps delay in the TPVs, and the simulations indicate a wide open eye.

I. Introduction

Two major applications are driving the need for low loss and high frequency interposers, (a) high bandwidth in 2.5D and 3D logic-memory and multi-memory architectures to achieve 28.8 Gbps and 56 Gbps high speed channels, and (b) mm-wave modules operating at 28 GHz, 39 GHz and other spectrum bands for future 5G mobile networks. Both these applications require ultra-low electrical loss and high precision circuits with high speed signal propagation and high density interconnections. 2.5D and 3D Silicon interposers, using through silicon vias (TSVs), face severe technical challenges including high electrical loss in large body sizes, and high cost, thus limiting their widespread commercial use. Glass has been proposed to be a superior alternative to silicon because of its excellent electrical property and the scalability to large panel sizes leading to lower cost [1].

The two key building block technologies required for glass interposers are fine pitch through package vias (TPVs) and re-distribution layers (RDLs). This paper presents detailed electrical modeling, design and characterization of TPVs in 300 μm thick 3D glass interposers, using a new high-throughput drilling technique, namely the focused electrical discharge method, capable of high throughputs, greater than 1000 vias per second [2]. The focused electrical discharge method is viewed to be a major enabler for high-performance glass interposers, since it is capable of forming high aspect-ratio TPVs at fine pitch with smooth side wall surfaces, unlike other approaches. There is limited literature about the high frequency electrical behavior of such TPVs in glass, and this paper represents the first comprehensive modeling and characterization study of high aspect-ratio TPVs in glass using the electrical discharge method for forming vias.

Five parameters are necessary to comprehensively evaluate the transmission performance with such TPVs: series resistance, series inductance, insertion loss, delay and eye diagrams. While the electrical performance of glass TPVs, formed by excimer laser ablation has been characterized [3], TPVs drilled by the focused electrical-discharge method have yet to be evaluated. Though the short-circuit-and-open-circuit method is not accurate, in the case of through-silicon-vias (TSVs) due to the electrical lossiness of silicon [4], it is the preferred method to extract the series resistance and inductance of TPVs in glass due to its simplicity and miniaturization, compared to other two-port measurement techniques requiring a large-area embedded capacitor [5]. The dual-via-chain method is the common method of choice to evaluate the insertion loss, but has only been applied so far up to 10 GHz [3, 6], which is insufficient for high-speed applications. Furthermore, the delay and the eye diagram of TPVs formed by the focused electrical-discharge method have not been investigated so far.

In this paper, two specific TPV configurations were designed and implemented in 300 μm thin glass interposers to fully assess the electrical performance of 55 μm diameter TPVs drilled by the focused electrical-discharge method up to 30 GHz. The first configuration was based on the short-circuit-and-open-circuit method, by which the series resistance and inductance of a single via can be retrieved from the Z-parameter that is calculated using the measured S-parameter. The second configuration was the commonly-used dual-via chain with long 50 Ω lines for insertion loss, delay and eye diagram. The insertion loss was measured up to 30

GHz by a Vector Network Analyzer (VNA) with excellent correlation of measured results to those from the 3D electromagnetic (EM) solver-Computer Simulation Technology (CST), while the delay and the eye diagram were generated using the simulated data in CST.

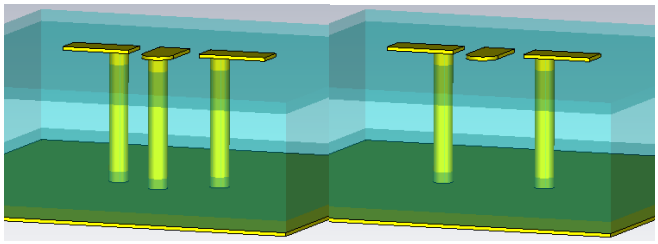
In Section II, the detailed high-frequency modeling and design are described. Then, the characterization data on the fabricated test vehicles is presented in Section III. Finally, the analysis and discussion of the results and the conclusions are given in Section IV and Section V, respectively.

II. High-Frequency Modeling and Design

The through package vias in the glass interposer can either be used for power and ground connections or signal transmission. The short-circuit-and-open-circuit method is an accurate technique to extract the series resistance and inductance for the power and ground TPVs, and the dual-via-chain method is widely used to characterize signal transmission TPVs. In this section, the modeling and the design for both methods are presented.

A. Short-Circuit-and-Open-Circuit Method

The short-circuit-and-open-circuit method was initially proposed in [4] to characterize the series resistance and inductance of TSV. The structures based on this methodology are shown in Fig. 1, including one structure that has a TPV shorting the signal to the backside ground and another structure that has identical dimensions but no shorting TPV for de-embedding the parasitic capacitance and conductance. The backside ground is constructed to be a plane rather than a trace, in that a ground plane has negligible inductance for perfect shorting. On the other hand, the probing pad is minimized to reduce the pad-introduced inductance.



(a) (b)

Figure 1. (a) Short-circuit structure shorted at the backside for retrieving resistance and inductance. (b) Open-circuit structure for de-embedding parasitic capacitance and conductance.

Based on this physical structure of Fig. 1(a), an equivalent circuit model can be derived, which is shown in Fig. 2. There are a total of three TPVs in this scenario, namely two ground TPVs and one signal TPV, where each TPV is modelled as a resistor in series with an inductor. For the Ground–Signal–Ground (GSG) probe, one signal pad and two ground pads are directly on the three TPVs, and parasitic capacitance and conductance respectively denoted by C and G in Fig. 2 exist between them, which can be de-embedded by the open-circuit structure.

Due to the symmetry of the GSG configuration, the current flowing through each of the two ground TPVs is estimated to be half of that in signal TPV. In other words, it is reasonable to assume that

$$\begin{aligned} L &= 2 \cdot L^* \\ R &= 2 \cdot R^* \end{aligned} \tag{1}$$

where L and R are the inductance and the resistance of the signal TPV respectively, while L^* and R^* are the inductance and the resistance of one ground TPV respectively.

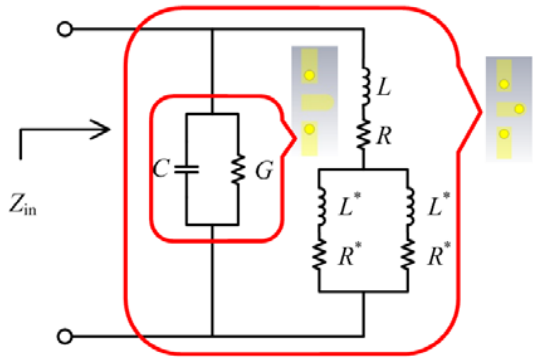


Figure 2. Equivalent circuit model of the short-circuit structure with the open-circuit structure included.

The input impedance of the short-circuit structure can be derived from the equivalent circuit model, which is

$$\frac{1}{Z_{in}} = j\omega C + G + \frac{1}{j\omega L + R + \dfrac{j\omega L^* + R^*}{2}} \tag{2}$$

where $\omega = 2\pi f$ is the radian frequency.

B. Dual-Via-Chain Method

A dual via chain is widely used to study the transmission performance of TPVs, which consists of one set of TPVs transiting from top to bottom and another set of TPVs transiting from bottom back to top, as shown in Fig. 3.

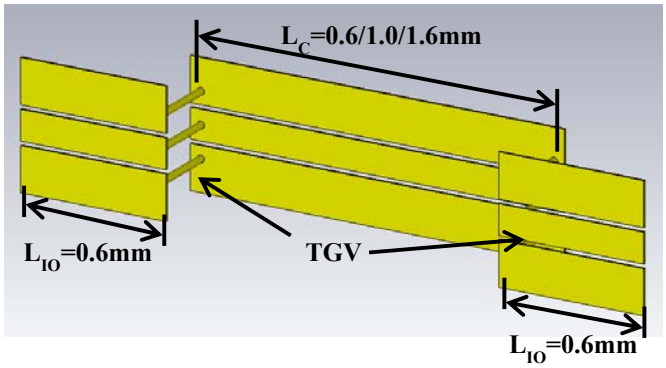


Figure 3. Dual via chain structure for studying the transmission performance of TPVs.

To support the GSG probes, co-planar waveguide (CPW) lines were applied and designed for 50 Ω matching. According to the stack-up shown in Fig. 4 and the electrical property of EN-A1 glass from Asahi Glass Company (AGC) [2] and ZEONIF™ ZS-100 polymer from Zeon Cooperation (Zeon) [7] listed in Table I, a 50 Ω CPW line was designed with the center conductor width of 141.025 μm and the gap between conductors of 20 μm. The length of the bottom connection lines was varied as L_C=0.6 mm, 1 mm and 1.6 mm, and the top CPW lines were fixed to L_{IO}=0.6 mm.

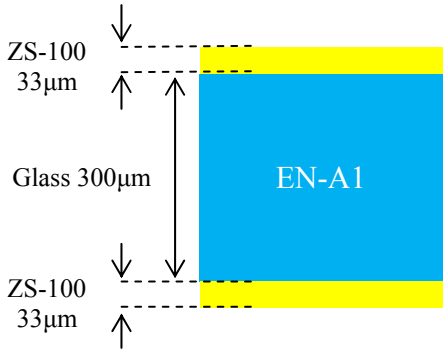


Figure 4. Cross-section view of the stack-up.

TABLE I
MATERIAL PROPERTY

Electrical Property	AGC EN-A1	Zeon ZS-100
Dielectric Constant at 10 GHz	5.46	3.0
Loss Tangent at 10 GHz	0.0056	0.005

The delay of the structure shown in Fig. 3 has three segments: the delay τ_{IO} from the top L_{IO} line, the delay τ_{TPV} from the TPV buried in the glass and the delay τ_C from the bottom L_C line. Then, the total delay of the whole structure can be expressed as

$$\tau = 2 \cdot \tau_{IO} + 2 \cdot \tau_{TPV} + \tau_C \quad (3)$$

Thus, the delay caused by the TPV can be captured by deducting the delay τ_{IO} and the delay τ_C from the total delay τ.

III. Characterization Results

Based on the modeling and design structures presented in the previous section, a test vehicle was fabricated using 300 μm AGC EN-A1 glass and 33 μm Zeon ZS-100 polymer, which is shown in Fig. 5. The TPVs were formed by the electrical-discharge method developed by Asahi Glass Company, with a 55 μm via diameter and 150 μm minimum center-to-center via pitch.

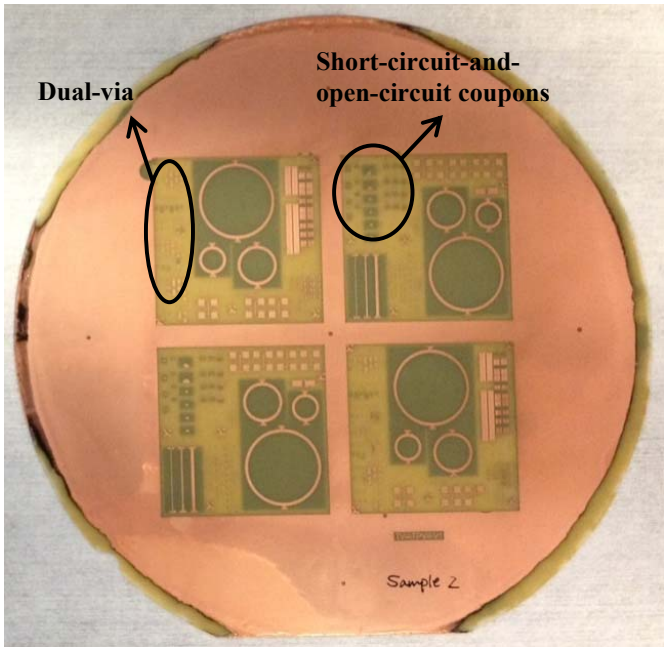


Figure 5. Top view of the fabricated test vehicle.

An on-wafer probe was used to measure the S-Parameters from 100 MHz to 30 GHz with an Agilent 8510C VNA and Cascade Microtech Ground–Signal–Ground (GSG) probes.

A. Results by Short-Circuit-and-Open-Circuit Method

TPVs should have no resistance or inductance in an ideal case. From the perspective of the impedance Smith Chart shown in Fig. 6, the ideal TPV is supposed to be located in the leftmost point of the impedance Smith Chart. Unfortunately, there is series resistance with each TPV because of the finite copper conductivity. Also, due to the skin effect, the input impedance moves from the outermost circle into the inside of the impedance Smith Chart. More importantly, the inductance effect introduced by the physical length of the TPV plays a critical role for high-speed digital applications, which might cause current overshooting. This inductance effect makes the input impedance travel along the outermost circle. Thus, the skin effect and the inductance effect of the TPV result in the impedance moving along the impedance Smith Chart to the inside.

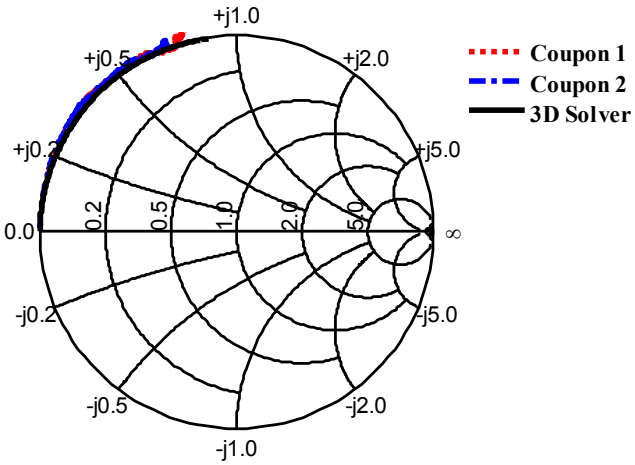
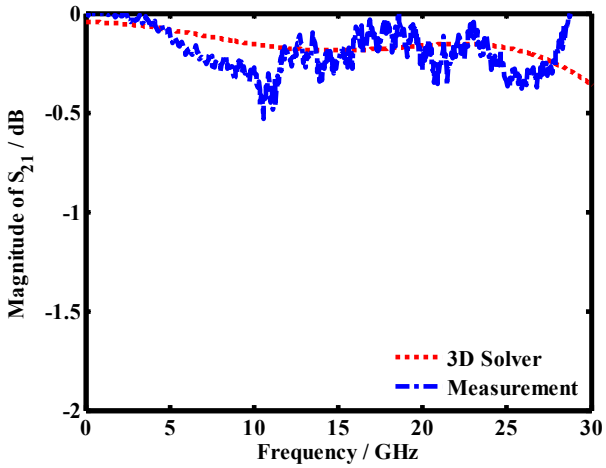
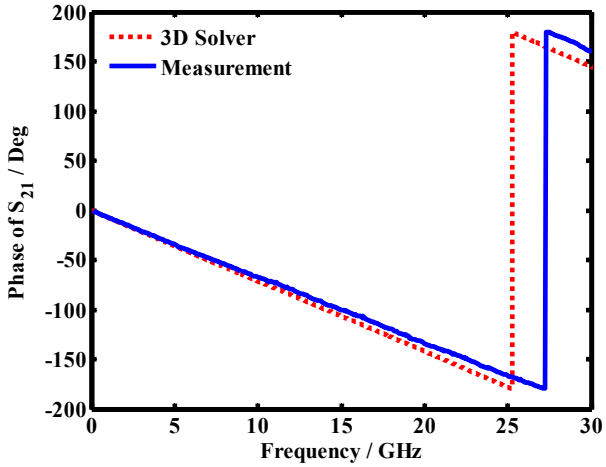


Figure 6. Measured and simulated results shown in the Impedance Smith Chart.



(a)



(b)

Figure 7. Comparison of the measured and simulated results: (a) the magnitude of S_{21} in dB; (b) the phase of S_{21} in Degree.

Two coupons with the same via location were measured up to 30 GHz, and the measured results are depicted in Fig.6 with the simulated results for comparison. It can be seen that the simulated results agree well with the measured results and more detailed interpretation of the data will be presented in the next section.

B. Results by Dual-Via-Chain Method

Three dual via chains were designed and implemented with different lengths, and the longest one had a total length of 2.8 mm excluding the length of the TPV. All these three lines were characterized up to 30 GHz. It is well known that the insertion loss increases with line length. Thus, the simulated and measured results of the longest chain are presented in Fig. 7, which shows excellent match between the simulated and measured results. The measurements demonstrate the superior electrical transmission of the TPV in the glass interposer, compared to TSVs. More analysis of the data will be provided in the next section to discuss the delay and the eye diagram for high-speed digital applications.

IV. Analysis and Discussion

In this section, detailed analysis of the results by the short-circuit-and-open-circuit method will be presented first. The extracted resistance and the inductance over a wide frequency range will be given, and the skin effect and the proximity effect will be discussed. Then, the delay profile as frequency and the eye diagram were generated using 3D EM solver – CST, based on the dual-via-chain method.

A. Results by Short-Circuit-and-Open-Circuit Method

The S-Parameters were measured using Agilent 8510C VNA and Cascade GSG probes. Once the S-parameters were obtained, they were converted into Z-parameters. Since these structures are a one-port network, the obtained S-parameter is essentially the return loss (Γ), which is related to the Z-parameters by the following equation [8]

$$Z_{in} = \frac{1}{Y_{in}} = Z_0 \frac{1+\Gamma}{1-\Gamma} \tag{4}$$

Then, according to formula (2), the resistance and the inductance of each TPV were calculated, shown in Fig. 8 and Fig. 9, respectively.

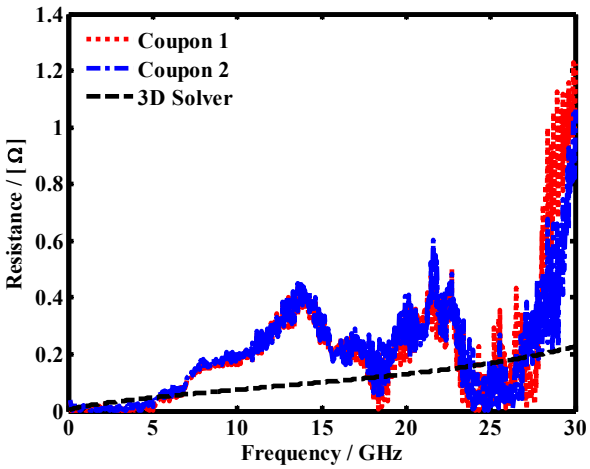


Figure 8. The resistance retrieved from the simulated and measured results.

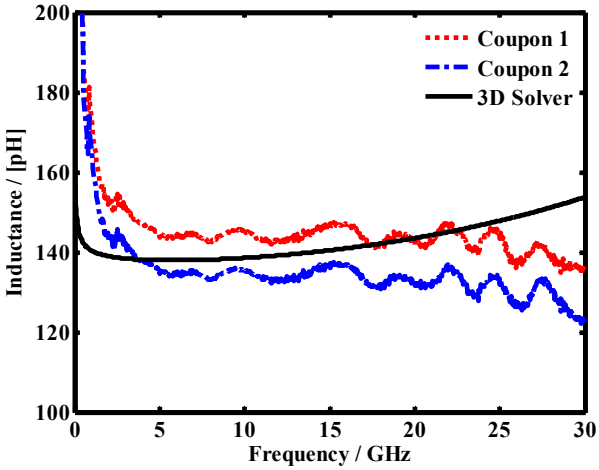


Figure 9. The inductance retrieved from the simulated and measured results.

In Fig. 8, it can be seen that the resistance of a single TPV is small and very challenging to measure. At 10 GHz, the simulated resistance was around 100 mΩ, which is close to the measured resistances with an average value of around 185 mΩ. Due to the skin effect, the resistance increases as frequency increases. In addition, because the skin depth follows the square root of frequency, the resistance also has the same square root relation with the frequency.

The extracted inductance is plotted in Fig. 9, and the measured results match well with the simulations. The inductance of a single via was estimated to be 140 pH which is much lower than the typical values for wire-bond interconnects, generally in the nH order of magnitude. At low frequencies below 5 GHz, the inductance decreases with frequency, because the skin effect causes the TPV to lose its internal inductance. Then, the inductance remains almost constant till the parasitic capacitance comes into play and results in LC resonance.

There are minor mismatches between the measured results and the simulated results at the lowest and at the highest frequencies. The minor mismatch at the lowest frequency is because the inductance effect is not pronounced, which makes the measurement rather challenging; while the minor mismatch at the highest frequency is due to a capacitance shift caused by the fabrication. In addition to these, the proximity effect also increases the mismatch between modeling and measurement. The magnitude of the magnetic field around the TPV is shown in Fig. 10. According to the boundary condition of the magnetic field shown below

$$\vec{J}_S = \hat{n} \times \vec{H} \tag{5}$$

the current flowing in the signal via is almost uniformly distributed along the via circumference. However, it is not the case for the two ground vias, as shown in Fig. 10. The magnetic field is almost crowded in half of the ground via while the other half is not contributing much to the current conduction. In other words, the assumption made in (1) is good but not very precise, considering the proximity effect.

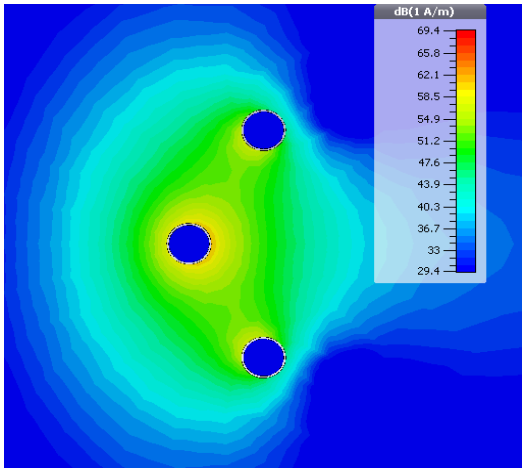


Figure 10. The magnitude of the magnetic field surrounding the TPV array.

B. Analysis of Dual-Via-Chain Results

Signal delay is a very important parameter for high speed digital applications, because it is critical for correct timing. Using the simulated results and the formula (3), all the delay profiles including that of the TPV were computed, and presented in Fig. 11. It can be seen that the total 6.2 ps delay of the TPV in glass is longer than that of the 0.6 mm long CPW line and it is close to the delay of the 1.6 mm long CPW line, though the physical length of the TPV is very short. This is due to the higher effective permittivity in the glass than in the CPW line. However, the delay of a typical TSV in silicon will be larger than that of TPV in glass, because the electrical permittivity of silicon – 11.9 is larger than that of glass – 5.46. Thus, TPVs in the glass interposer can support faster transistor speed than TSVs.

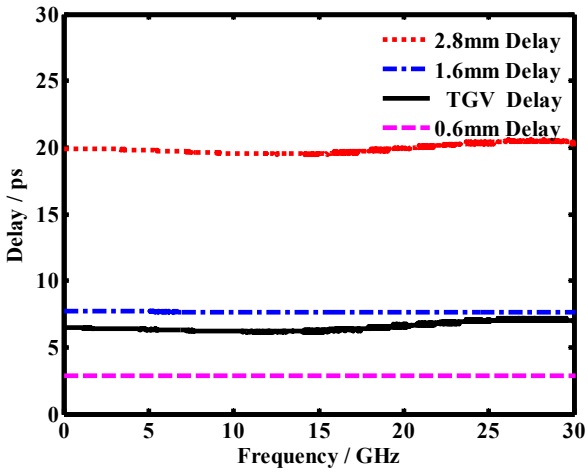


Figure 11. All the delay profiles generated by the simulated results from CST.

Fig. 12 shows the eye diagram obtained in 3D EM Solver - CST, for a 20 Gbps pseudo-random bit stream (PRBS) transmitted through a dual via chain (shown in Fig. 3) with the bottom CPW line length set at 1.6 mm. It can be seen that the eye is clearly open with 1.43 mV jitter, 50 ps eye width and 0.91 V eye height.

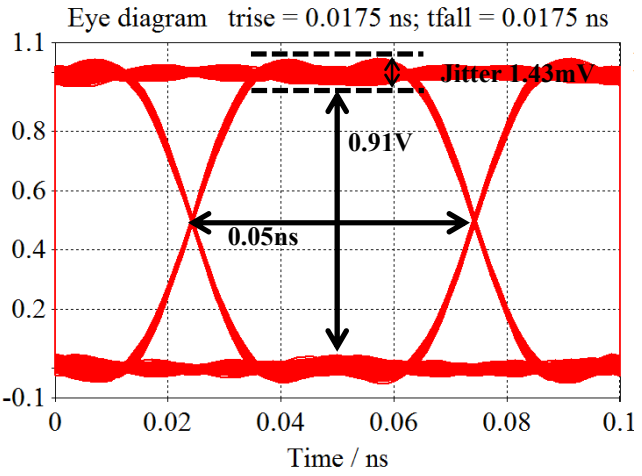


Figure 12. The simulated eye diagram at 20 Gbps for 2.8 mm glass CPW channel.

V. Conclusions

A detailed electrical modeling, design and high frequency characterization, up to 30 GHz, was presented for high aspect-ratio 55 µm diameter TPVs in 300 µm thin glass, formed by a novel focused electrical discharge method that is capable of greater than 1000 vias per second throughput. Such a glass interposer is ideal for 2.5D and 3D package integrations for two major applications: high performance digital systems with high logic-memory bandwidth, and mm-wave modules at 28 GHz and higher frequencies for future 5G mobile networks. The high-aspect-ratio and smooth-side-wall TPVs drilled by the focused electrical discharge method, produce exceptionally low resistance and inductance, and achieved high-quality signal transmission enabled by low loss and delay, even at high frequencies. These results establish the superior electrical performance of glass interposers with such TPVs, thus making glass the ideal package material for high-speed digital and 5G mobile systems.

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