Finite Element Analysis and Experiment Validation of Highly Reliable Silicon and Glass Interposers-to-Printed Wiring Board SMT Interconnections

Xian Qin, Nitesh Kumbhat, Pulugurtha Markondeya Raj, Venky Sundaram, and Rao Tummala

Abstract—Interposers that support high input/output density are becoming critical for system miniaturization and high performance. Silicon and glass are emerging as the primary candidates for such high-density interposers, due to their outstanding dimensional stability, which enables layer-to-layer wiring with small vias. However, silicon and glass have very low coefficients of thermal expansion (CTE), 3–8 ppm/°C, compared with organic printed wiring board (PWB), which has a CTE of 12–18 ppm/°C. The large CTE mismatch between interposer and board raises reliability concern with the ball grid array interconnections. In this paper, compliant dielectric build-up layers laminated on silicon and glass interposers are explored as stress buffers to reduce the strain accumulated in solder interconnections. Finite element method was used to analyze the thermo-mechanical reliability of the interconnections, and predict the fatigue life of solder joints. Three types of low-CTE interposer materials were studied, low-CTE glass (3 ppm/°C), high-CTE glass (8 ppm/°C), and silicon (2.7 ppm/°C). Test vehicles with the above three interposers at a size of 7.2 mm × 7.2 mm with 25-µm-thick polymer stress buffers laminated on both sides were fabricated, and assembled on organic FR-4 boards using Sn96.5Ag3Cu0.5 solder. The reliability of the solder interconnections, with the three different test vehicles, was studied using thermal cycling test from −40 °C to 125 °C. The high-CTE glass sample was observed to survive 1800 thermal cycles before the first failure was detected in one of the corner joints. Experimental results of fatigue life of interconnections agreed well with finite element modeling results, and reliable interconnections between low-CTE interposer and organic PWB using stress buffers were demonstrated. Based on the validated model, parametric study was conducted to explore the influence of geometry and material properties of interposer on the thermo-mechanical reliability of the solder interconnections, as a guideline for interconnection design of similar interposers.

Index Terms—Compliant dielectric, finite element method, model validation, reliability test, thin silicon or glass interposer.

I. INTRODUCTION

ORGANIC materials are most commonly used for today’s packaging substrates. They are easily processable and cost efficient. However, organic substrate systems are known to have poor dimensional stability, which limits their miniaturization, as well as through vias pitch and reliability for high density interconnections. Silicon and glass interposers or packages are being explored as the next generation substrates to address the limitations of organic substrates [1]. These interposers have excellent dimensional stability, thus allowing ultrahigh input/output density interposers. However, they raise reliability concerns when directly assembled on printed wiring boards (PWBs), due to the large mismatch in coefficient of thermal expansion (CTE) between the interposers (3–8 ppm/°C) and PWBs (12–18 ppm/°C).

Traditionally, the interconnection between interposer and PWB is achieved using eutectic tin-lead (SnPb) solders, as they exhibit good mechanical properties and low-temperature processability. However, SnPb solders are being replaced by lead-free solders due to the environmental hazards and associated restrictions in the use of lead in solder alloys. Most of the lead-free solders are known to be less ductile and more prone to fatigue under aggressive thermo-mechanical loading [4], further aggravating the reliability concerns in ball grid array (BGA) interconnections. When lead-free solders connecting low-CTE interposer and organic PWB are subjected to power or thermal cycling, cyclic shearing stresses on solder joints will be created, leading to fatigue failure. Similar CTE mismatch related reliability issues have been solved in the past for silicon IC to organic package interconnections by a variety of methods, such as using underfills. However, underfilling is not an acceptable option for package-to-board interconnections, because it does not allow reworkability after assembly. Therefore, there is a need to investigate novel methods to address the surface mount technology (SMT) reliability challenges for such low-CTE interposers.

Literature reports multiple approaches to address the thermal expansion mismatch. Copper bump-based approaches were developed to replace the solders for chip-to-organic substrate interconnections at 100–200-µm pitch [5], [6]. However, they offer limited compliance if applied at the board level.
In this paper, compliant build-up dielectric layers laminated on glass and silicon interposers are proposed to decouple the stress between the interposer and PWB. This approach offers unique performance, cost, and processability benefits, not provided by the above approaches reported in literature. The 2-D plane strain models were built to analyze the thermo-mechanical reliability of solder interconnections and to validate the effectiveness of the proposed approach. The area-averaged equivalent plastic strain range in each loading cycle was used as the damage metric for fatigue life prediction. Glass and silicon interposers (7.2 mm × 7.2 mm), laminated with a polymer (RXP-4M) as stress buffer, were fabricated, and assembled onto PWB with 400-μm pitch interconnections. The 2-D finite element models were developed to study the reliability of low-CTE interposer to PWB and interposer with a size of 7.2 mm × 7.2 mm. The schematic of such an interposer is shown in Fig. 1(a). The shear strain in solder is reduced in the presence of a compliant polymer layer, as shown in Fig. 1(c), since part of the CTE mismatch is accommodated by shear deformation of the polymer stress buffer layer. Therefore, there is a decrease in the damage in solder caused by cyclic thermo-mechanical loading. The low-cycle fatigue of lead-free solders can be characterized by Coffin-Manson relationship

\[ N_f = 0.5 \left( \frac{2\varepsilon_f}{\Delta\gamma P} \right)^{-1/c} \]  

where \( N_f \) is the number of cycles to failure, \( \Delta\gamma_p \) is the cyclic plastic strain range, \( \varepsilon_f \) and \( c \) are material-related constants. Equation (2) shows that smaller shear strain in the solders leads to longer fatigue life, which validates the use of polymer stress buffer to improve the reliability of BGA interconnections.

II. Finite Element Modeling

The polymer stress buffer layer accommodates the CTE mismatch by shear deformation, as shown in Fig. 1. Fig. 1(a) shows the stress-free state of the assembly. During reflow process, there is no induced stress in the solder when it is still in liquid state. Stress is induced in solder interconnections as the temperature drops below the eutectic temperature of the alloy, as solidification occurs. When the assembly is cooled down to room temperature at the end of reflow, solder deformation occurs due to the CTE mismatch between the board and the interposer, as shown in Fig. 1(b). The shear strain of solder is proportional to the difference in CTE between the interposer and the board, as shown in (1), where \( L_{DNP} \) is the distance to neutral point, \( \Delta T \) is the temperature variation from stress free temperature, \( h_j \) is the height of the joint, \( \alpha_{PWB} \) and \( \alpha_{Pac} \) are the CTE of the PWB and the interposer, respectively

\[ \Delta\gamma = \frac{L_{DNP}(\alpha_{PWB} - \alpha_{Pac})\Delta T}{h_j}. \]  

Symmetric boundary condition was applied on the left boundary condition of the structure, therefore all the nodes on this boundary are neutral points with no displacement along the horizontal direction. The bottom point of the left boundary was pinned to avoid free body movement. Lead-free solder SnAgCu (SAC305) was chosen as the solder material. The viscoplastic property of SAC305 was captured with Anand model, using the nine Anand constants from [13].
Bilinear kinematic hardening elastic-plastic property was used for copper and the other materials were modeled as linear elastic. The material properties are shown in Table I. The assembly was subjected to a temperature drop from stress free temperature (217 °C) to room temperature (25 °C), simulating the SMT process, followed by five thermal cycles each from 125 °C to −40 °C. The equivalent plastic strain range per cycle in solder was calculated to assess the reliability of interconnections and predict the fatigue life.

### III. Modeling Results and Fatigue Life Prediction

Fig. 3 shows the contour plot of equivalent plastic strain in solders in a high-CTE glass to PWB assembly at the end of five thermal cycles. A maximum nodal strain of 8.75% was found in the corner solder. The corner solder has the largest distance to neutral point compared with the inner solders, resulting in the largest strain range and damage in each thermal cycle. Therefore, it can be expected that the failure will initiate from the corner solder and propagate toward the inner solders.

Similar models without the compliant stress buffer layers were built as a baseline to evaluate the effectiveness of the stress buffer approach. Same geometrical parameters, material properties, boundary, and loading conditions were applied. The geometry is shown in Fig. 4. In the model where high-CTE glass was used as the interposer material, the maximum nodal strain in the solder was 9.99% at the end of five thermal cycles, which is higher compared with 8.75% when stress buffer layers were applied.

Several damage metrics have been previously reported for life prediction of lead-free solders, such as accumulated plastic strain per cycle, plastic strain range per cycle, accumulated creep strain per cycle, strain energy density per cycle, creep strain energy per cycle, and so on [14]. In this paper, the equivalent plastic strain range in each thermal cycle was chosen as the damage metric. An area average method was used to get the critical strain for life prediction. The strain was averaged over four elements in the vicinity of the location where the largest nodal strain happens, as shown in Fig. 5. Similar analysis was conducted for solder joints connected to low-CTE glass and silicon interposers. The first time to failure was considered as fatigue life of the interconnection, and was calculated using (2), where the material constants εf and c equals 0.325 and −0.57, respectively [17]. The calculated critical strain and fatigue life of solder interconnections with different interposers are shown in Table II. Similar calculation was conducted for the models where no stress buffers were applied, and the strain and fatigue life are calculated. Compared with the baseline model, the fatigue life of the interconnections can be improved by 11.3%–18.4% by applying the stress buffer layers.

### IV. Test Vehicle Design and Fabrication

A 90° rotation symmetric design was used for the test vehicle. There are 12 daisy chains in each interposer-to-board assembly. The daisy chains at the four corners [daisy chain No. 1, 4, 7, and 10 in Fig. 6(a)] are most likely to fail, since they are furthest from the neutral point. The other eight daisy chains were interconnected, since the failure possibility...
Fig. 4. Baseline model. (a) Geometry: high-CTE glass to PWB interconnection without applying stress buffer layers. (b) Nodal equivalent plastic strain in solders at the end of five thermal cycles.

Fig. 5. Selection of elements for average strain calculation.

is relatively smaller, and monitored as a single daisy chain for efficient testing.

Test vehicles were fabricated with three different interposer materials: 1) high-CTE glass; 2) low-CTE glass; and 3) silicon. The thickness of both high-CTE glass and low-CTE glass was 180 μm, and the thickness of silicon was 240 μm. A 25.4-μm-thick dry film polymer (RXP-4M) was used as the stress buffer. Both sides of the interposer were laminated with stress buffer layer to maintain balance and prevent warpage. The interposer was then metalized using electroless and electrolytic copper plating. Electroless nickel, electroless palladium, and immersion gold were used as the surface finish. SAC305 solder ball attachment was then performed on one side of the interposers. The solder ball diameter was 250 μm, and the ball pitch was 400 μm. The interposers were diced and assembled on FR-4 board for testing. Fig. 6(b) shows the schematic of assembled test vehicles.

V. RELIABILITY TESTS AND RESULTS

Thermal cycling test (JESD22-A104D, type G) was carried out to investigate the reliability performance of interconnections with high-CTE glass, low-CTE glass, and silicon-based interposers assembled on PWB. The temperature extremes were −40 °C and 125 °C, respectively. The soak time was 10 min at both the temperature extremes, and the ramp rate for temperature transition was 15 °C/min. The resistance of each daisy chain in the test vehicles was recorded every 100 cycles to test the electrical integrity of the interconnections, and the normalized resistance of the four corner daisy chains and the combined daisy chains was plotted for each test vehicle.

Based on electrical resistance measurements, high-CTE glass test vehicle was found to survive 1800 cycles before the first failure as shown in Fig. 7(a). There was a significant increase in the resistance of the corner daisy chain two between 1800 and 1900 cycles, while the resistance of other daisy chains remained relatively constant. In the low-CTE glass test vehicle, initial failure was found at one of the corner daisy chains at 1300 cycles while other daisy chains were still intact, as shown in Fig. 7(b). With the silicon test vehicle, as shown in Fig. 7(c), the first failure was found in one of the corner daisy chains after 300 cycles. At the end of 700 cycles, eight out of the 12 daisy chains had failed.

In all the three test vehicles, the first failures occurred in the corner daisy chains consistent with the modeling results. The high-CTE glass sample showed maximum reliability due to minimum CTE mismatch between the interposer and the board. The low-CTE glass has a higher CTE (3.8 ppm/°C) compared with silicon (2.7 ppm/°C), which explains the better reliability performance compared with silicon interposer.

The test vehicles that exhibited failures were cross-sectioned for failure analysis. Fig. 8 shows the cross section of silicon test vehicle after 710 cycles. From cross-sectional analysis, the central solder joints were found to be intact, while the edge joints displayed cracks on the interposer side.

After the initial failure found at 1900 cycles in the high-CTE glass test vehicle, thermal cycling was continued to 2400 cycles for significant development of cracks. Based on cross-sectional analysis after 2400 cycles, shown in Fig. 9, the cracks had propagated through the corner solder joint,
TABLE II
CRITICAL STRAIN AND FATIGUE LIFE PREDICTION OF SOLDER INTERCONNECTIONS—WITH AND WITHOUT STRESS BUFFERS

<table>
<thead>
<tr>
<th>Interposer material</th>
<th>With/ without stress buffer</th>
<th>Area averaged equivalent plastic strain range per cycle</th>
<th>Fatigue life</th>
<th>Improvement compared to baseline model</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-CTE glass</td>
<td>With</td>
<td>0.0053642</td>
<td>2260</td>
<td>14.3%</td>
</tr>
<tr>
<td></td>
<td>Without</td>
<td>0.00579</td>
<td>1976</td>
<td></td>
</tr>
<tr>
<td>Low-CTE glass</td>
<td>With</td>
<td>0.00836062</td>
<td>1037</td>
<td>18.4%</td>
</tr>
<tr>
<td></td>
<td>Without</td>
<td>0.0092</td>
<td>876</td>
<td></td>
</tr>
<tr>
<td>Silicon</td>
<td>With</td>
<td>0.01054764</td>
<td>690</td>
<td>11.3%</td>
</tr>
<tr>
<td></td>
<td>Without</td>
<td>0.0112</td>
<td>620</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 6. Design and schematic of the test vehicle. (a) Daisy chain configuration of interconnections. (b) Cross-sectional schematic.

VI. VALIDATION OF FINITE ELEMENT MODELING—DISCUSSION

Table III shows the comparison of predicted fatigue life based on finite element modeling and the experimental results while crack initiation had begun in the neighboring solder joint. In both the cases, the cracks were found to be present along the intermetallic layer on the interposer side.

Fig. 7. Normalized daisy chain resistance change during thermal cycling of different test vehicle. (a) High-CTE glass. (b) Low-CTE glass. (c) Silicon (bigger image, one below the other).
for all three types of test vehicles. The modeling results for both the high-CTE and the low-CTE glass interposer agreed well with the experimental results, with a variation of fatigue life within 20%. Significant deviation between modeling and experiment was observed for silicon interposer test vehicle.

A possible explanation for the deviation could be that the silicon panel used in the experiment is substantially thicker (240 μm) than that in modeling (180 μm). Using classic laminate theory, assuming same Poisson’s ratio for substrate and dielectric materials as an approximation, the effective CTE of the interposer with polymer laminated on both sides can be estimated by the following equation [18]:

$$a_{equ} = \frac{2E_1\alpha_1 + nE_2\alpha_2}{2E_1 + nE_2} \quad (3)$$

where $n$ is the thickness ratio of substrate over dielectric layers, $E_1$ and $\alpha_1$ are the modulus and CTE of the dielectric, $E_2$ and $\alpha_2$ are the modulus and CTE of the substrate. Therefore, the effective CTE of the interposer is a weighted average of the CTE of the substrate material (silicon, in this case) and the polymer material. The CTE mismatch between the interposer and board reduces with increasing, decreasing the thermo-mechanical loading on the solder. As the thickness of the silicon panel increases, the thickness ratio, $n$, in the equation also increases, leading to a decrease in effective CTE of the interposer, thereby resulting in more damage on the solder during thermo-mechanical loading.

Based on cross-sectional analysis, the failure was found to initiate in the corner solder on the interposer side for all three test vehicles. However, from modeling results, the highest nodal strain was predicted on the board side, since the top side is connected directly to the stress buffer layers. Two considerations may have accounted for this inconsistency. First, as seen in Fig. 8, the solder resist opening on the interposer side is smaller than that on the board side leading to a smaller contact area and weaker bonding on the interposer side. Another factor could be that the solder ball was first attached on the interposer side and then assembled on the board. As a result, the solder on the interposer side was reflowed twice. During reflow, the intermetallic compounds (IMCs) at the copper pad-solder interface coarsen rapidly and the IMC layer grows in thickness [19]. Extensive IMC growth deteriorates the reliability of the solder interconnection due to the brittle nature of the IMCs [20]. Thicker IMC layer on the interposer side weakens the bonding and favors crack initiation, thereby making it a preferential site for failure.

The results indicate that the modeling showed consistent results with the experiments with some deviations possibly due to processing and material-related issues that were not taken into consideration in the models. Further parametric analysis based on finite element modeling was carried out to explore the effect of interposer size and dielectric material properties on the thermo-mechanical reliability performance of the interconnections, as a design guideline to further improve interconnection reliability.
TABLE III
FATIGUE LIFE FROM MODELS AND EXPERIMENTS

<table>
<thead>
<tr>
<th>Interposer type</th>
<th>Fatigue life</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Calculated from models</td>
</tr>
<tr>
<td>High-CTE glass</td>
<td>2260</td>
</tr>
<tr>
<td>Low-CTE glass</td>
<td>1037</td>
</tr>
<tr>
<td>Silicon</td>
<td>690</td>
</tr>
</tbody>
</table>

- **Fig. 10.** Warpage contour of silicon interposer at the end of five thermal cycles.

- **Fig. 11.** Effect of interposer size on warpage—high-CTE glass interposer.

VII. PARAMETRIC ANALYSIS BASED ON FINITE ELEMENT MODELING

A. Effect of Interposer Size on Warpage

At the end of five thermal cycles, the interposer warps downward in a convex shape, as seen in Fig. 10. The maximum displacement in the y-direction is 23.4 μm at the furthest solder joint for a 7.2-mm × 7.2-mm size silicon interposer connected to PWB with 400-μm pitch BGA.

As the size of interposer increases, the distance between furthest solder balls to the neutral point becomes larger, as well as the warpage. Fig. 11 shows the warpage of high-CTE glass interposer with increasing interposer sizes. It can be observed that the warpage increases significantly with the increase in interposer size, following a parabolic shape. The same trend has been observed for models with different interposer materials. At 7.2-mm × 7.2-mm size, the warpage of high-CTE glass interposer is 17.6 μm, smaller than that of silicon interposer (23.6 μm) with the same size (Fig. 10). Li [21] studied die warpage dependence on die size in a flip chip package, and observed a similar trend. For a 10-mm × 10-mm silicon die connected to organic package with underfill, warpage of 140 μm was reported, in comparison to 59 μm, when a silicon interposer of same size is connected to PWB with stress buffer layers in this paper. The large warpage reported in [21] is partially due to the low standoff height of the flip chip interconnections, and the application of underfill.

B. Effect of Interposer Size on Interconnection Reliability

The maximum equivalent plastic strain in interposers with different sizes was calculated and shown in Fig. 12. When the interposer size is smaller than 6 mm × 6 mm, the plastic strain accumulated in solders during thermal cycles increases dramatically with the increase in interposer size. The curve levels off after the interposer size increases beyond 6 mm. However, it cannot be concluded that the thermo-mechanical reliability of the solder interconnections will remain the same regardless of the increase in interposer size. As shown previously in Fig. 11, the warpage of the interposer increases parabolically with size, and the large warpage results in large von Mises stress in the interposer, as well as large in-plane compressive stress in the solder, as shown in Fig. 13(a) and (b). It has been reported that compressive stress leads to out-diffusion of copper and surface metallization into solder, and facilitates IMC growth [22]. Hence, it can be estimated that the fatigue life of the solder interconnection will deteriorate as the interposer size increases, due to increase in the warpage and accelerated growth of IMC layer.
C. Effect of CTE of Dielectric on Interconnection Reliability

Dielectric materials with different CTEs were used in the model, and the equivalent plastic strains at the end of thermal cycles in solders for each scenario were compared. Young’s modulus of the dielectric material was fixed at 1.3 GPa to simplify the analysis. As seen from Table IV, higher CTE of the dielectric material helps to reduce the plastic strain accumulated in the solders. As evident from (3), higher CTE of the stress-buffer increases the effective CTE of the interposer, thereby generates lower CTE mismatch.

D. Effect of Dielectric Layer Modulus on Reliability

The effect of modulus of the dielectric layer on the reliability was studied by changing the modulus from 1 MPa to 5 GPa while keeping the other parameters constant. A CTE of 45 ppm/°C was chosen for this analysis. The corresponding maximum equivalent plastic strain in solders is shown in Fig. 14. It is observed that the equivalent plastic strain in the solders does not change monotonously with dielectric modulus.

When the modulus of dielectric layer is sufficiently low, the interposer is effectively decoupled from the PWB by the dielectric layer, and the CTE mismatch is mainly accommodated by the shear deformation of laminated polymer layers. The shear strain in dielectric layers is shown in Fig. 15. High shear strain was found in the areas connected to solder balls. Lower modulus effectively reduces the accumulated plastic strain in the solders during thermal cycles. Therefore, more CTE mismatch is accommodated by the dielectric layers, leading to larger shear strain as shown in Fig. 16.

With higher modulus of dielectric layer, the substrate cannot be effectively decoupled from the board; therefore, the elastic
deformation of dielectric layer is limited. From (3), it can be seen that the effective CTE of the sandwiched interposer is a function of both the CTE and the modulus of the dielectric material. As the modulus of the dielectric material increases, the CTE of the composite structure (package with dielectric layers) also increases. The resulting higher CTE of the interposer translates to a lower CTE mismatch between the interposer and the board, which explains the reduction in solder strain with respect to increasing modulus of the stress buffer. As a result of these opposing trends, the change in behavior of equivalent plastic strain in solder balls with respect to the modulus of the dielectric layers for these models was found to be \( \sim 700 \text{ MPa} \). The exact transition point requires a more detailed study as it is sensitive to the mesh density used in the modeling. Below the transition point, stress buffer material with lower modulus and higher CTE is expected to effectively decouple the interposer from the board, thereby improving the fatigue life.

Based on the above analysis, the stress buffer material with suitable modulus and CTE can be chosen to provide adequate reliability for an interposer with given body size and required interconnection fatigue life. At a given thickness, the stress buffer with the combination of lowest available modulus and highest CTE is expected to provide the highest reliability. Such a stress buffer also defines the largest CTE mismatch and body size that can be accommodated by this approach. When the use of thicker stress buffer material is allowed, reliable interconnection can be achieved for interposer with lower CTE and larger body size.

### E. Effect of Through Vias

The above discussion is based on one metal layer structure without through interposer vias. To investigate the effect of through vias on the interconnection reliability, vias filled with copper were included in both the models with and without the stress buffer layers. The geometry and nodal equivalent plastic strain for both cases are shown in Fig. 17. The via diameter was 72 \( \mu \text{m} \), and for simplification, no buffer material was applied on the sidewall of the vias. In the model without stress buffer layers, incorporation of through silicon vias reduced the solder strain by 10%, from 0.099 to 0.089. The high CTE of copper (17.3 ppm/\(^\circ\)C) contributed to the higher composite CTE of the interposer (glass and copper vias as a whole), and thereby lower CTE mismatch with the PWB. Zhang et al. [24] also reported a reduction in the creep strain energy density per cycle in the BGA solder bumps by through silicon vias in the silicon interposer.

With the compliant stress buffer material applied, the maximum nodal strain reduced to 0.074, while without stress buffer layers, the strain was 0.089. Therefore, the stress buffer layers are shown to provide additional reduction in the solder strain even when there are through vias in the interposer. Compared with the strains showed in Figs. 3 and 4, the strains in solder
have reduced for both the structures with and without stress buffer layers.

VIII. CONCLUSION

In this paper, compliant dielectric material was explored to efficiently decouple the resultant stress in solder interconnections from the CTE mismatch between low-CTE interposers to PWB. The reliability of 400-μm pitch BGA interconnections between thin glass and silicon interposers to PWBs was studied using finite element modeling and thermal cycling test with prototype test vehicles. The high-CTE and low-CTE glass test vehicle did not exhibit failures up to 1800 and 1300 cycles, respectively, demonstrating excellent reliability with the dielectric approach.

The fatigue life of both high-CTE and low-CTE glass test vehicles was found to be consistent with modeling predictions. Significant deviation was observed in case of silicon interposer, however, because of the larger thickness of silicon interposer used in the fabrication. Further parametric study was conducted based on the validated models to investigate the influence of interposer size and stress buffer material properties on interconnection reliability. Combining the modeling results, solder microstructure evolution and material property transitions, it can be concluded that interposers with lower CTE and larger body size present a larger challenge to interconnection reliability. It can also be found that dielectric materials with low modulus (lower than the transit point from modeling) and high CTE are effective stress buffers.

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