

Silicon & Glass Interposer (SiGI)

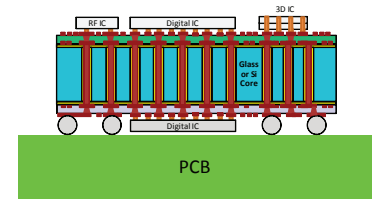
Low-Cost, Panel-Based Silicon and Glass Interposer (SiGI) for Packaging of ULK ICs and 3D ICs

What

- Panel-based glass and silicon packages with 20-50 μ m pitch to interconnect 2D ICs with ULK and 3D ICs at \sim 10X lower cost than wafer-based silicon interposers

Why

- ULK ICs and 3D ICs need packages with low CTE, very high I/Os at very small pitch and at very low cost
- Si interposers address this need but are expected to be too expensive on cost per I/O basis for some applications
- Organic packages are reaching limits in I/O density, thermal and cost per I/O



Georgia Tech PRC Proposal

Georgia Tech proposes panel-based glass and silicon packages to address the above by:

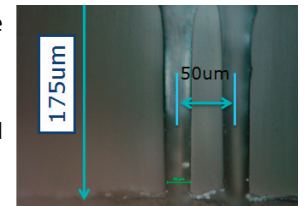
- Demonstration of \sim 5X improvement in I/O density at \sim 10X lower cost
- Addressing two major barriers: 1) low cost TPVs and 2) improved thermal conductivity
- Extending these packages with minimum re-distribution layers, embedded thin-film components, and SMT reliability to organic boards

Unique Features of this Global Consortium Include:

- Focus on low cost high I/O packages – 8X reduction from larger panels, 2X reduction from package materials and processes
- Address fundamental barriers to use of glass – form TPV holes at much lower cost than TSV, and improve its thermal conductivity
- Develop high throughput processes for vias, wiring and interconnections
- Focus on high interconnection reliability and high yield
- Develop both panel and wafer-compatible processes
- Clear path to commercialization through key IDM and supply chain partners

Research Focus

- Electrical and thermo-mechanical design
- Ultra-thin, large-area and low-cost silicon and glass substrate materials
- Low-cost through-package-via (TPV) materials and processes
- Low-cost and high I/O double-sided interconnections
- Package to PWB Interconnection materials, processes and reliability
- Thermal conductivity improvements
- Embedded thin film components



Research Tasks and Team

Program Manager – Dr. Venky Sundaram

- **Electrical & Mechanical Design** – Mr. Tapo Bandyopadhyay, Mr. Vivek Sridharan, Mr. Srikrishna Sitaraman, Mr. Qiao Chen, Ms. Xian Qin, Mr. Gokul Kumar, Mr. Nitesh Kumbhat, Prof. Sung-Kyu Lim, Dr. Raghu Pucha, Prof. Suresh Sitaraman, Prof. Madhavan Swaminathan
- **TPV in Glass and Silicon** – Mr. Vijay Sukumaran, Mr. Qiao Chen, Mr. Yoichiro Sato (Asahi Glass Co.)
- **High I/O Wiring** – Dr. Fuhun Liu, Mr. Vivek Sridharan, Mr. Vijay Sukumaran, Mr. Qiao Chen, Mr. Yuya Suzuki (Zeon Corporation)
- **IC-Package-PWB Interconnections** – Mr. Nitesh Kumbhat, Dr. Raj Pulugurtha, Mr. Dibyajat Mishra, Ms. Xian Qin
- **Embedded Components** – Dr. Raj Pulugurtha, Dr. Himani Sharma, Mr. Vivek Sridharan
- **Thermal Management** – Prof. Yogendra Joshi, Dr. Raj Pulugurtha
- **Demonstrator** – Mr. Vijay Sukumaran, Mr. Qiao Chen, Mr. Tapo Bandyopadhyay, Mr. Vivek Sridharan, Dr. Venky Sundaram, Mr. Nitesh Kumbhat, Dr. Fuhun Liu
- **Industry Liaison and Memberships** – Mr. Dean Sutter, Director of Operations
- **Faculty Director** – Prof. Rao Tummala, Center Director

Phase II

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Website:

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