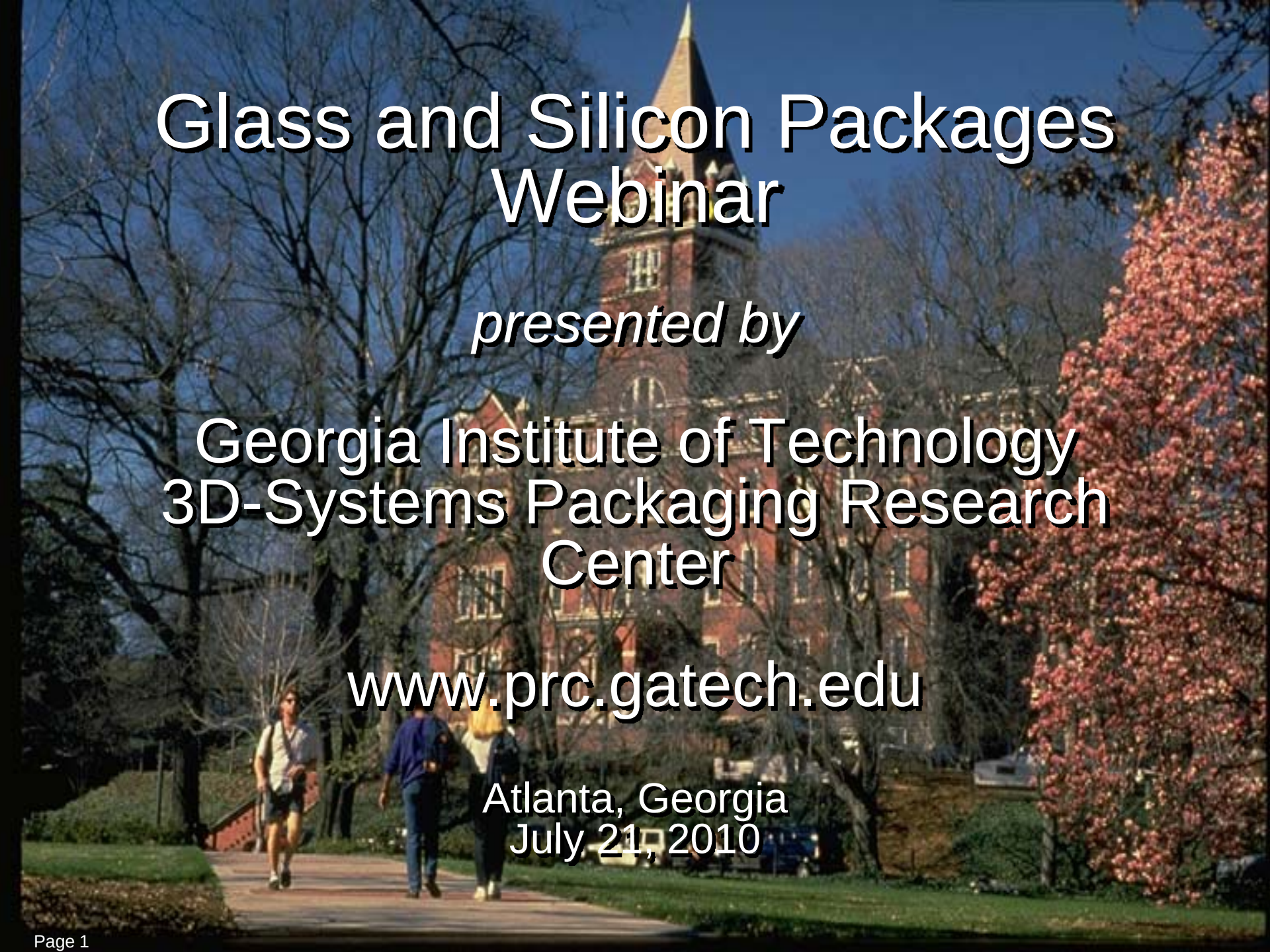

Glass and Silicon Packages Webinar
presented by
Georgia Institute of Technology
3D-Systems Packaging Research Center
Webinar will begin at 12:00 p.m. EDT



Glass and Silicon Packages Webinar

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Georgia Institute of Technology
3D-Systems Packaging Research Center

www.prc.gatech.edu

Atlanta, Georgia
July 21, 2010

Webinar Outline

- Introduction – Prof. Rao Tummala
  - Purpose of Webinar
  - What are glass and Si packages?
  - Why panel-based glass and Si packages?
  - Cost factors and applications
  - Potential markets for glass and Si interposers
- Phase 1 Program Details – Dr. Venky Sundaram
  - Objectives
  - Glass and Silicon Package Concept
  - Research targets, tasks and team
  - Uniqueness of Georgia Tech
  - Companies interested, membership options and costs
  - Next step for Companies and for Georgia Tech

Purpose of Webinar

- Invite Global Electronic Companies to Join GT PRC Consortium either as “Full Member” with IP rights or as “Supply Chain Member” to supply glass or silicon panel materials, tools, substrates, packages or modules:
  - For strategic technology
  - To leverage company funding by 10X
  - Utilize Industry-centric and proven team

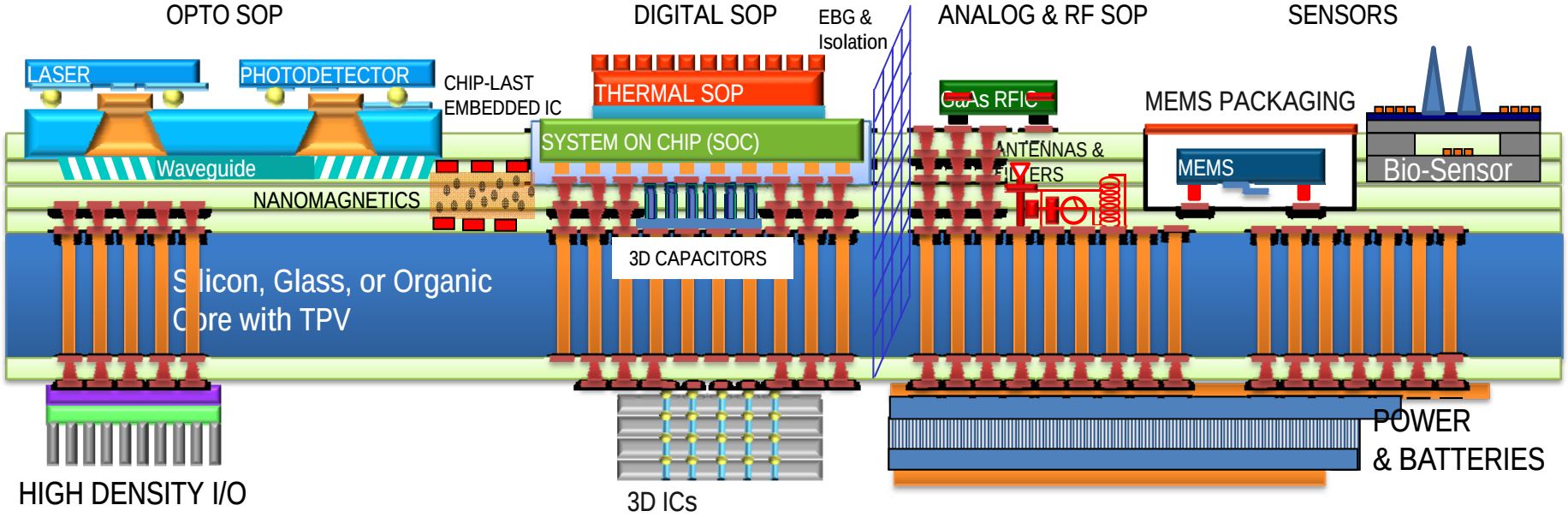
PRC Vision of SOP System

NANOMATERIALS

EMBEDDED COMPONENTS

INTERCONNECTIONS

SUBSTRATES & SYSTEM INTEGRATION



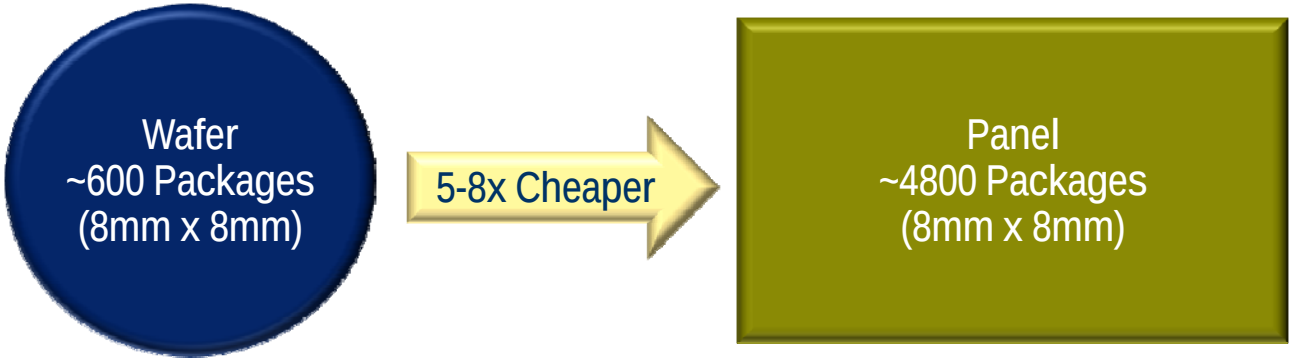
MIXED SIGNAL ELECTRICAL DESIGN

THERMAL

MECHANICAL DESIGN FOR RELIABILITY

What are Glass and Si Packages?

- Panel-based glass and silicon packages in contrast to wafer-based

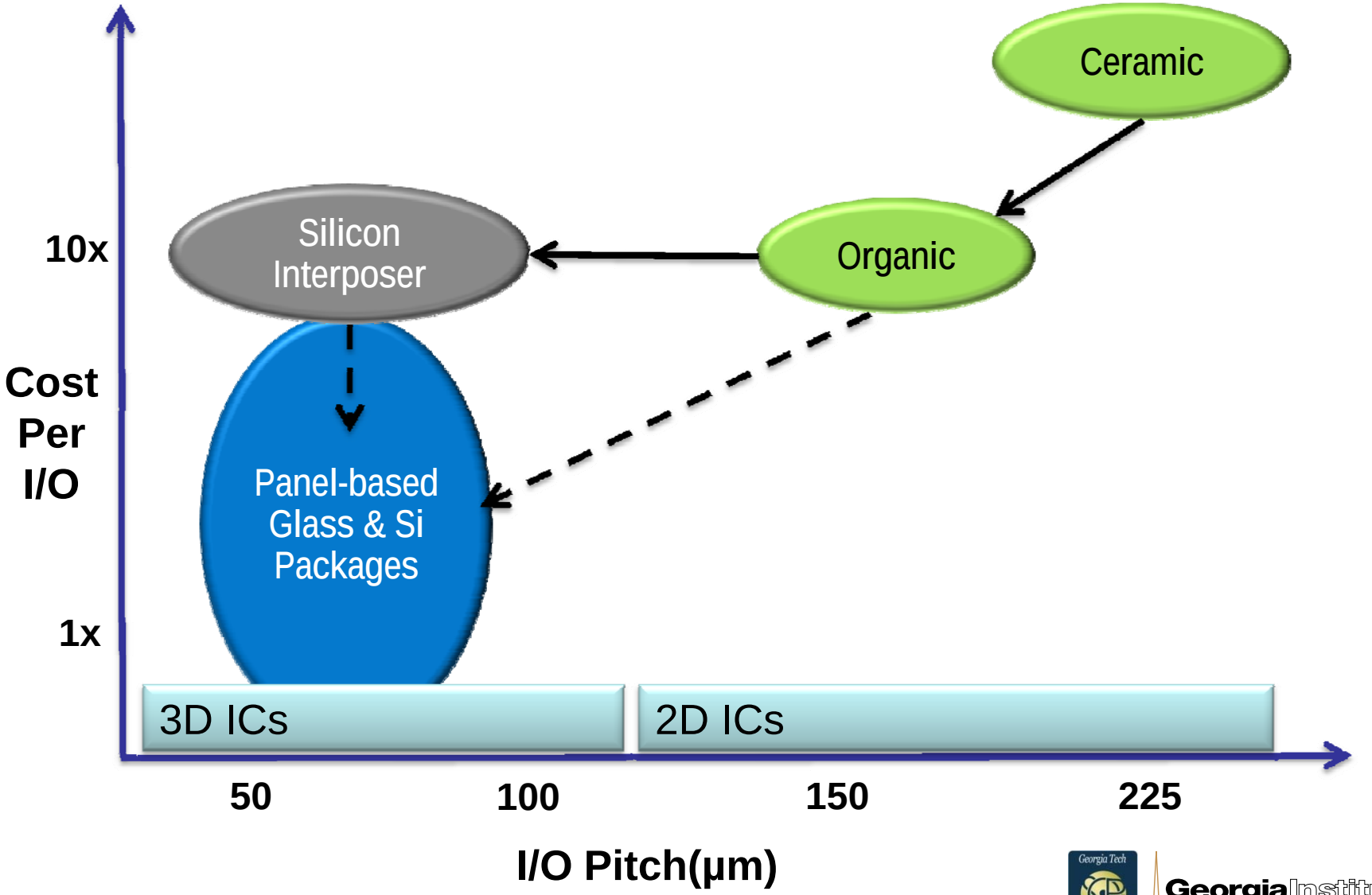


Wafer-based Silicon Interposers from 300mm Wafer

Proposed Glass and Si packages from 600mm Panel

- Why
  - ~10x Potential cost reduction from wafer-based silicon interposers (5-8x from panel size and 2x from materials and processes)
  - Basic technologies applicable to 300mm Si wafers

Why Panel-based Glass & Si Packages?



Ideal Properties of a Package Material

Characteristic	Materials				
	Ideal Properties	Glass	Silicon	Organic	Metal
Electrical	• High resistivity • Low loss				
Physical	• Smooth surface finish • Large area availability • Ultra thin				
Thermal	• High Conductivity • CTE matched to Si				
Mechanical	• High strength • High modulus				
Chemical	• Resistance to process chemicals				
Processability	• Ease of Via formation and metallization				
Cost	• Low cost per I/O at 25um pitch				

Good Fair Poor

Why Large Glass or Si panel?

Functions	Materials				
	Glass	Silicon		FR-4	Metal
		Wafer-based	Panel- Based		
Properties					
•Electrical	Insulator	Semiconductor	Semiconductor	Insulator	Conductor
•CTE Mismatch	Good	Good	Good	Poor	Good
•Dimensional Stability	Good	Good	Good	Poor	Good
Processability					
•Via Formation	Slow	Good	Good	Good	Fair
•Metallization	Simple	Complex	Complex	Simple	Complex
Cost					
•Raw Panel Cost I/O	Low	High	Medium	Low	High
•Processed Cost	Low	High	Low	Medium	High

Why Glass and Silicon Packages?

Feature	CURRENT Organic Approach	CURRENT Si Interposer	PROPOSED Large Si/Glass Approach
IC-to-Package I/O Pad Pitch	60-100µm	40um	20-50µm
Package Line Dimension	20 µm	1-5 um	1-5 µm
TCE Mismatch (IC-to-Package to PWB)	3 PPM vs. 17 PPM vs. 17 PPM	3 PPM vs. 3 PPM vs. 17 PPM	3 PPM vs. 3 PPM vs. 17 PPM
Dimensional Stability	Poor	Good	Good
Line Resistance (Ω/mm)	0.12 (15µm L/S, 10µm thick)	~0.4-2.0 (5µm L/S, 1-3µm thick)	~0.2-0.4 (5µm L/S, 8µm thick)
Cost – Panel / Wafer Size – Raw Core – cost/I/O@30µm Pitch	 – 600mm – Low – High	 – 200-300mm – High – High (BEOL process)	 – 600mm – Medium – Low (pkg process)

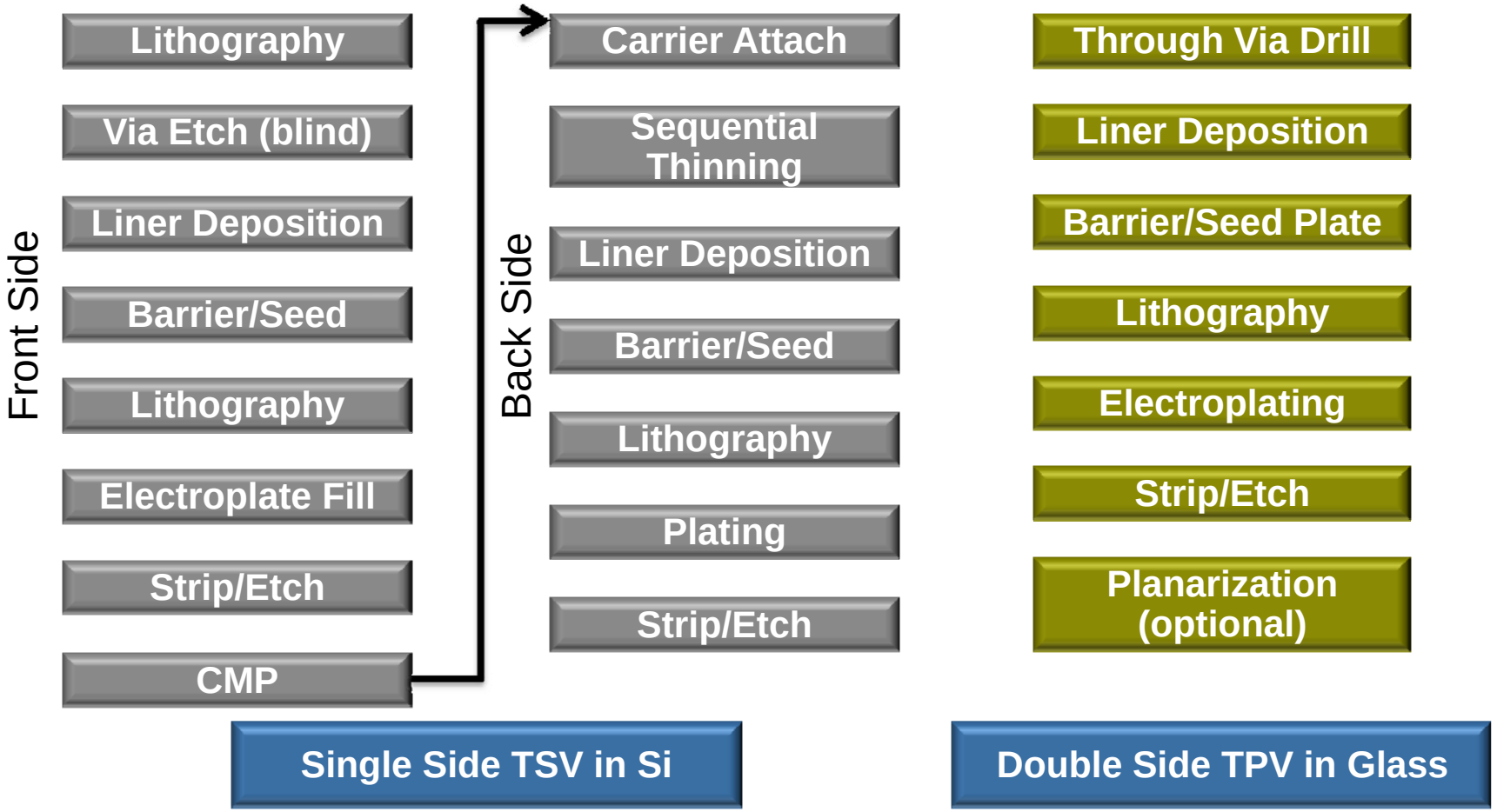
* Limitations Shown in Red

Cost Factors

- Size-driven cost factors
  - Panel Size vs. Wafer Size
- Material and process-driven cost factors
  - Process simplicity
  - Eliminate insulating liner
  - Lower cost package materials and processes
  - Minimum number of layers
  - Double side processing

Minimizing Process Steps

- Example of TPV process step reduction



Potential Markets for Glass/Si Interposers

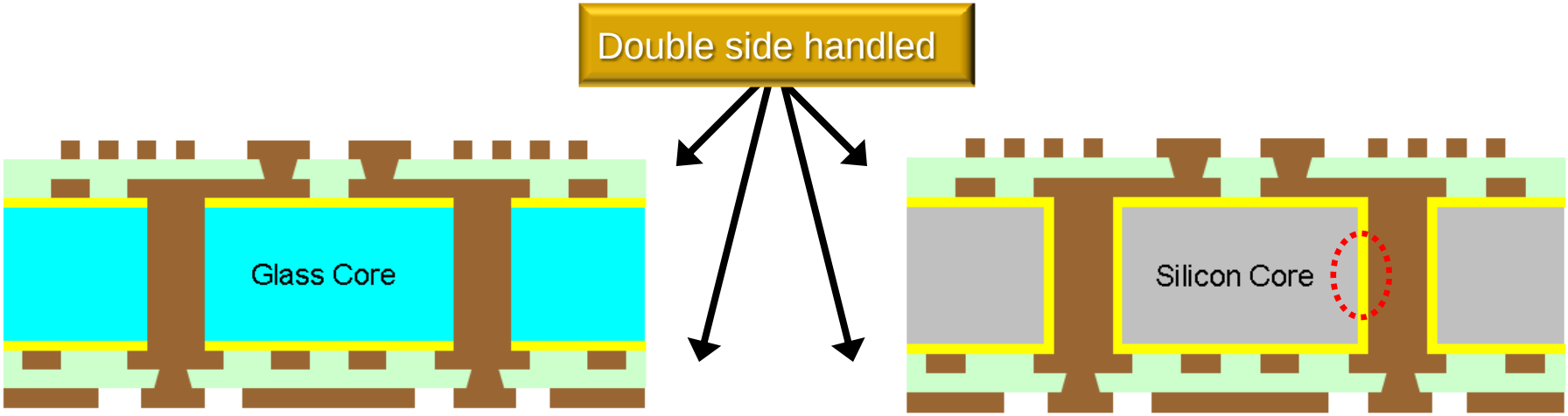
- Replacement of organic substrates for high I/O BGA
  - ~US$8B in 2008 – Source: JMS
- Integrated Passive Devices (IPDs) using thin film on glass/Si
  - ~US$1B by 2013 – Source: Yole Development
- 3D Interposers for, 3D ICs, SiP, RF Modules and other multi-chip packages
  - ~US$5B – Source: Yole Development
- 3D-WLP
  - ~US$6-7B – Source: Yole Development
- MEMS, optical and bio packaging with through glass vias (unique properties of glass critical for these applications)

PHASE 1 PROGRAM DETAILS –
DR. VENKY SUNDARAM

Phase 1 Objectives

- Electrical and mechanical design guidelines for TPV
- TPV Materials and processes in Glass and Si
  - 20-50µm diameter at 50-100µm pitch
- 5µm RDL Technology at 50µm pitch
- Reliable 1st level Cu bump interconnections
- Reliable 2nd level SMT interconnections to PWB
- Glass and Silicon package demonstrators

Research Targets



Physical Parameters

- TPV diameter: 10~50um
- Copper line width/spacing: 3~10um
- Glass or Si thickness: 100~300um
- Buildup thickness: 5~20um
- Copper thickness: 3~10um
- Via diameter: 15~25um

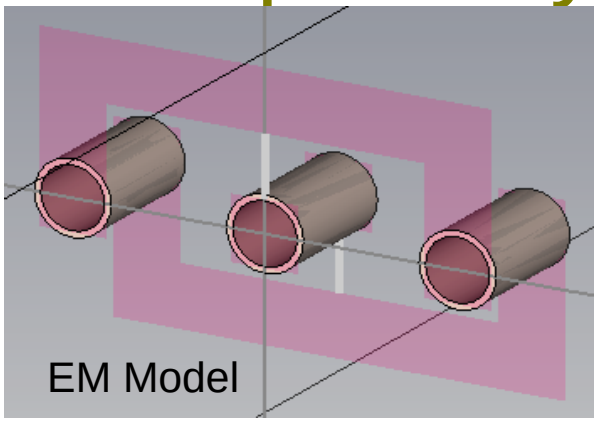
Electrical Parameters

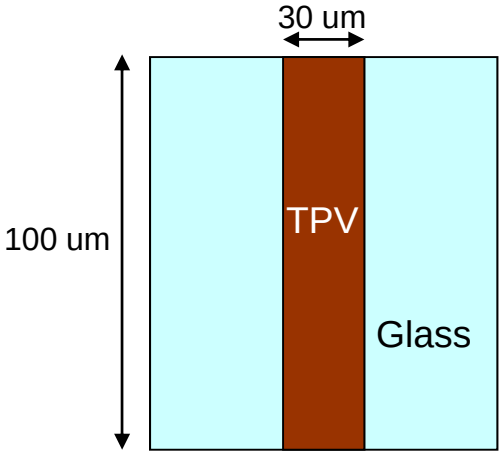
- Resistance (R)
- Inductance (L)
- Signal Transmission (Zo, Gamma)
- Coupling (K)

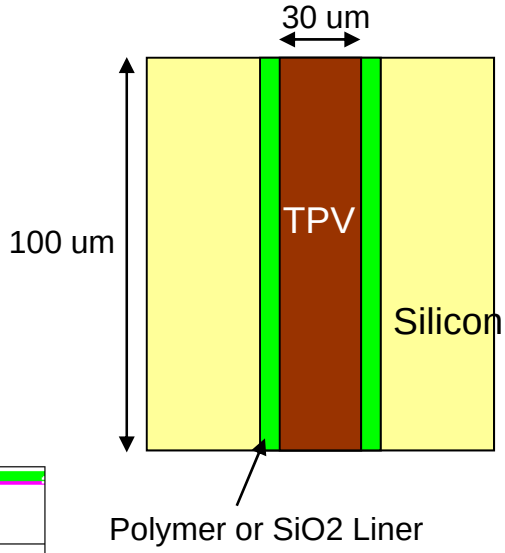
Research Tasks & Team

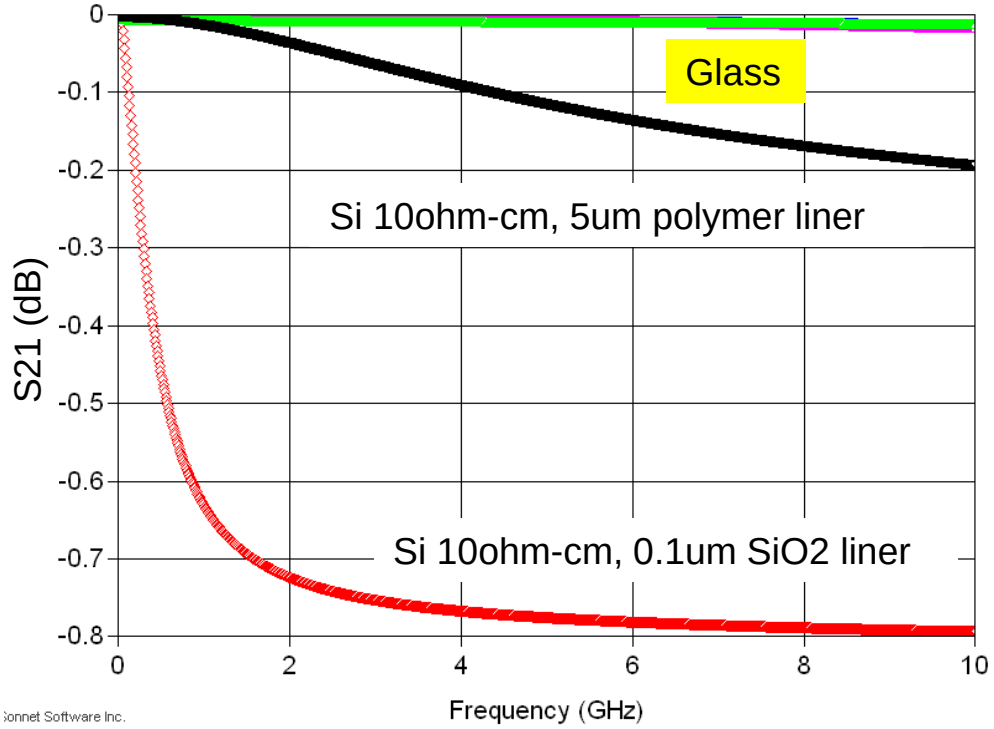
Task	Academic & Research Faculty / Students
Program Director	Dr. Venky Sundaram
Electrical & Mechanical Design	Mr. Tapo Bandyopadhyay, Mr. Vivek Sridharan, Mr. Qiao Chen, Mr. Nitesh Kumbhat, Dr. Raghu Pucha
TPV in Glass and Silicon	Mr. Vijay Sukumaran, Mr. Qiao Chen
High I/O Wiring	Dr. Fuhan Liu, Mr. Hunter Chan, Mr. Vivek Sridharan, Mr. Vijay Sukumaran, Mr. Qiao Chen
IC-Package-PWB Interconnections	Mr. Nitesh Kumbhat, Dr. Raj Pulugurtha
Embedded Components	Dr. Raj Pulugurtha, Dr. Himani Sharma, Mr. Vivek Sridharan
Thermal Management	Prof. Yogendra Joshi, Dr. Raj Pulugurtha
Demonstrator	Mr. Vijay Sukumaran, Mr. Qiao Chen, Mr. Tapo Bandyopadhyay, Mr. Vivek Sridharan, Mr. Hunter Chan, Dr. Venky Sundaram, Mr. Nitesh Kumbhat, Dr. Fuhan Liu
Industry Liaison & Memberships	Mr. Dean Sutter, Director of Operations
PRC Director	Prof. Rao Tummala

Superiority of Glass Over Silicon

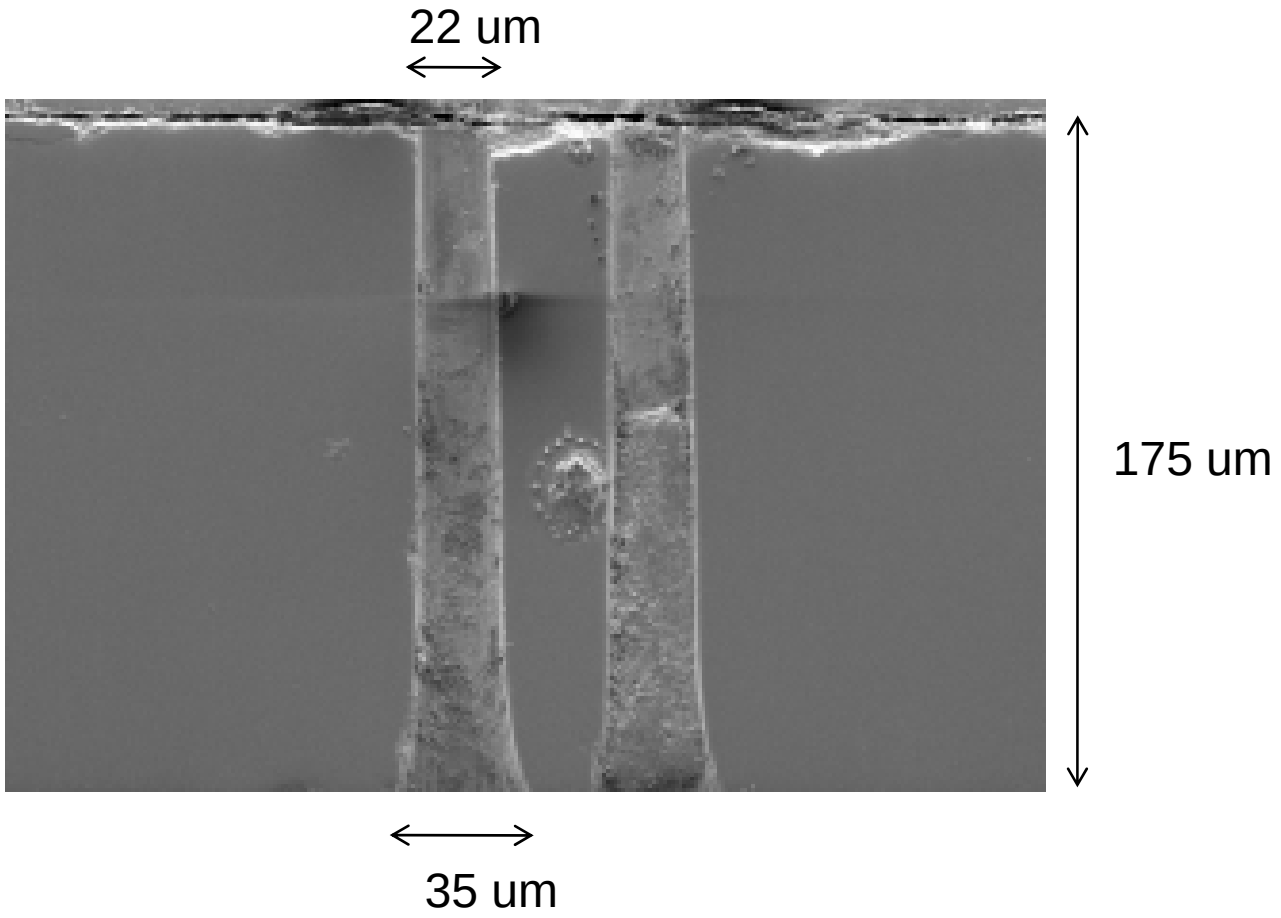






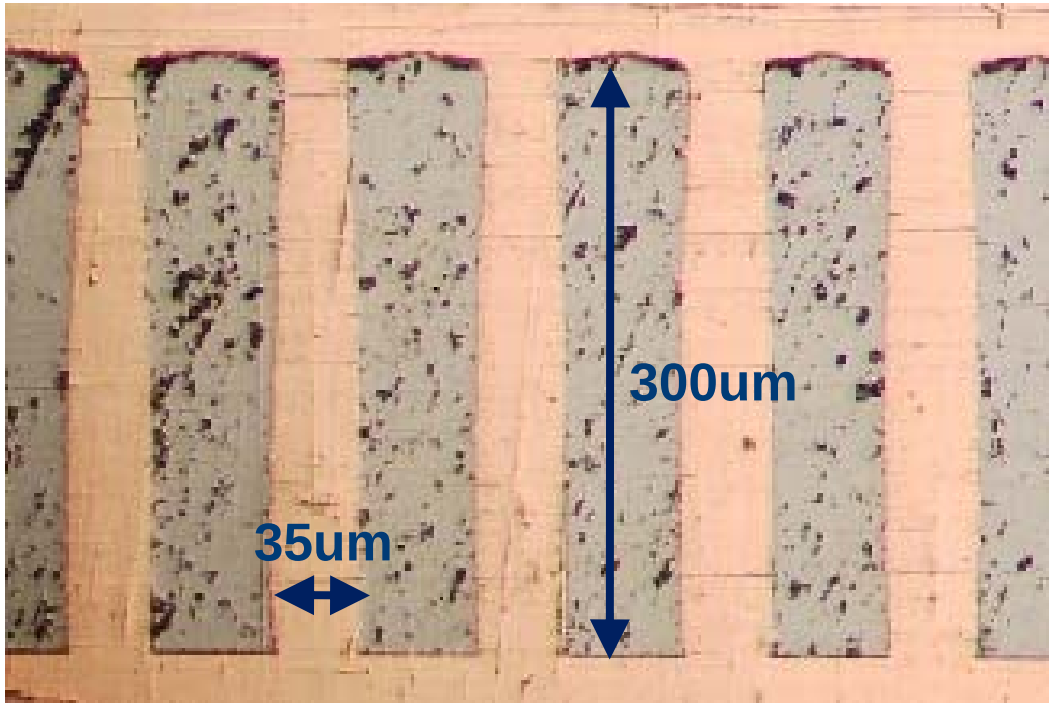


First demonstration of 50um pitch Through Package Via (TPV) in ultra-thin glass



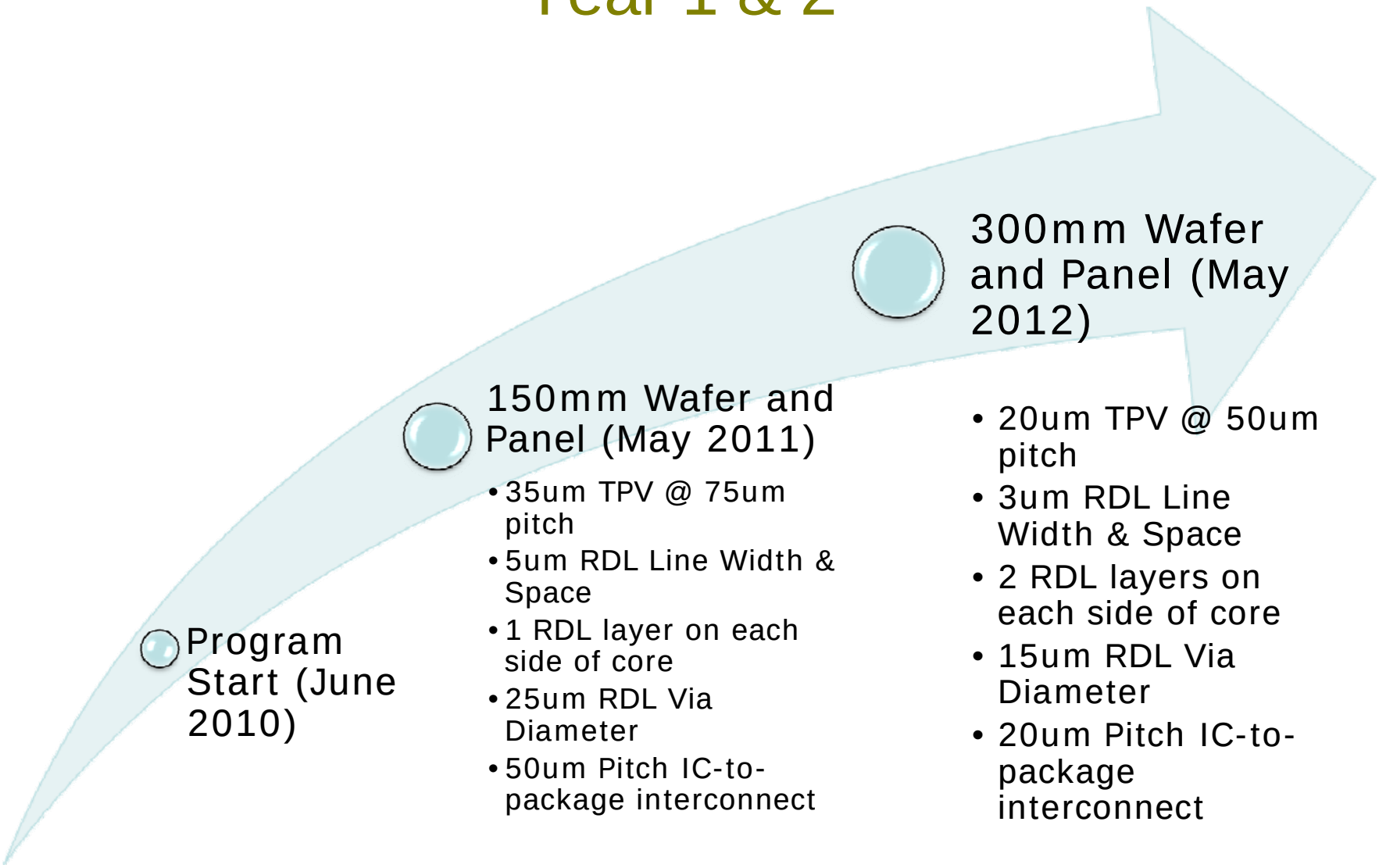
SEM of via cross-section

Double-Side Plated Through Package Via in Silicon Interposer



- 300um thick CMOS Si
- All double side processing (no handle wafer)
- High aspect ratio 10:1 to 15:1
- Void-free filling
- Cu burden removed by wet etch

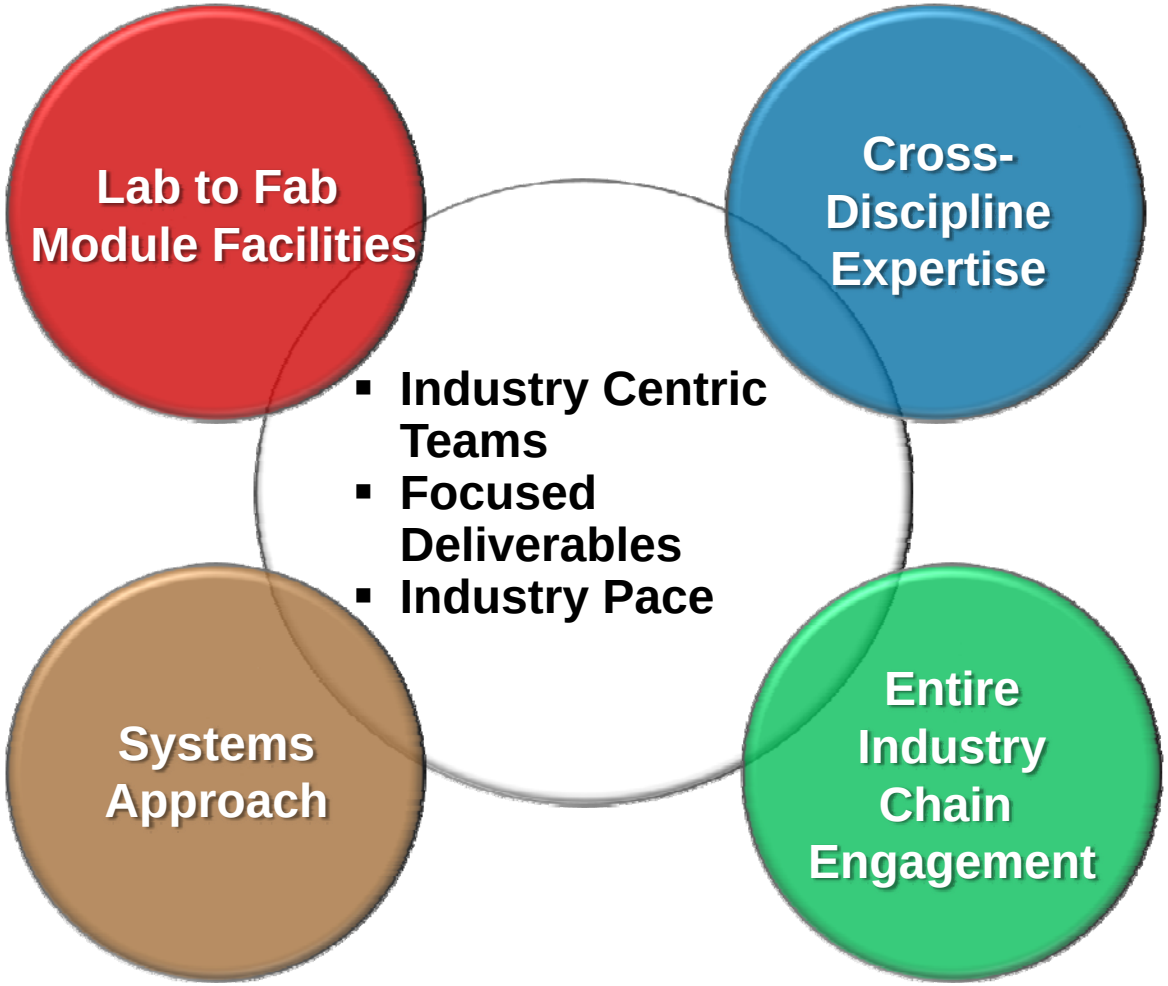
Deliverables Target for Si & Glass Package Year 1 & 2



Two Commercialization Paths for Technology Building Blocks

	Panel Based Package	Wafer Based Package
Manufacturing Size	450-600mm rectangular panel	300mm round wafer
Manufacturing Location	Extension of current organic interposer fabs	300mm wafer fab
Materials/Process	Dry film, laser, plating	Photo materials option
Tools	Combination of •Organic substrate tools (with upgrades) •FPD tools	Wafer level packaging and/or BEOL tool set with higher throughput
Unit form factor	Larger interposer sizes	Smaller interposer sizes
Cost per unit area	Lower	Low

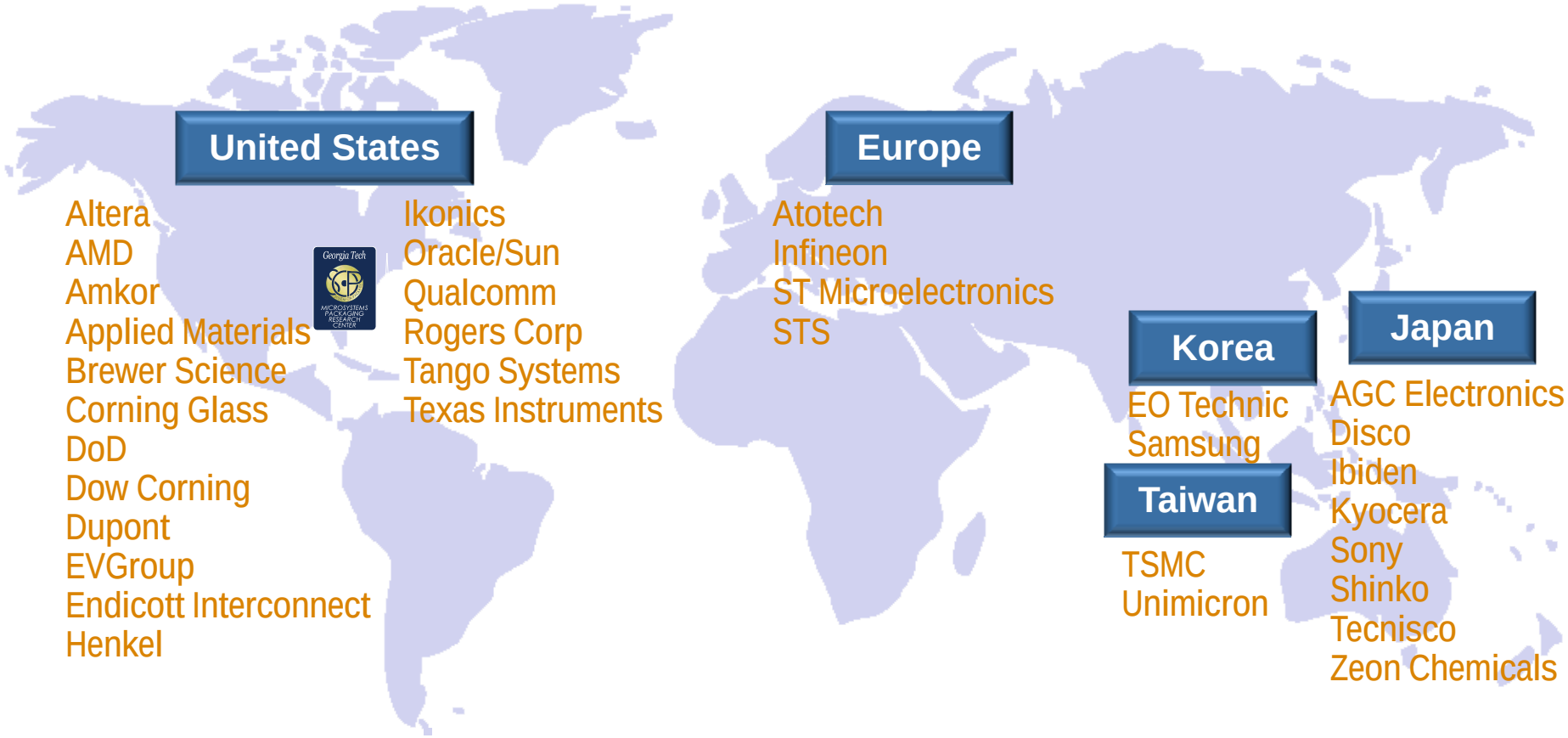
Uniqueness of 3D Microsystems Packaging Research Center



Consortia Membership Benefits

Benefit	Full Member	Supply Chain
• Annual Membership Cost	$100k	$25K
• Program/Project Mentor	Yes	No
• Program/Project Steering	Yes	No
• I/P Rights – N.E.R.F License	Yes	No
• I/P Test Vehicle Rights/Info	Yes/Yes	No/Yes
• Meeting Participation	Yes	Yes
• Reports	Yes	Limited
• Materials/Equipment in Program	Yes	Yes
• Engineer-on-Campus	Yes	Yes “In kind” Related
• Leveraging of GT Know How	Yes	Yes
• Leveraging of Membership $	Yes	Yes

Companies Interested in Glass/Si Packages Program at GT PRC



United States

Altera
AMD
Amkor
Applied Materials
Brewer Science
Corning Glass
DoD
Dow Corning
Dupont
EVGroup
Endicott Interconnect
Henkel
Ikonics
Oracle/Sun
Qualcomm
Rogers Corp
Tango Systems
Texas Instruments

Europe

Atotech
Infineon
ST Microelectronics
STS

Korea

EO Technic
Samsung

Taiwan

TSMC
Unimicron

Japan

AGC Electronics
Disco
Ibiden
Kyocera
Sony
Shinko
Tecnisco
Zeon Chemicals

Next Step for Companies

- Consortium launched June 2010
- Companies to select one Option
  - Full Member with IP rights
  - Supply Chain To supply to companies
- Companies with high interest
  - Will receive white paper
  - Customized scope for full members
  - Next Face to Face Meeting at GT: November 10-11, 2010
- Contact Persons:
  - Venky: vs24@mail.gatech.edu
  - Dean: dean.sutter@ece.gatech.edu
  - Prof Tummala: rtummala@ece.gatech.edu

Glass and Si Package Webinar

Thank you for joining us.

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