

# EMAP II Webinar

*presented by*

Georgia Institute of Technology  
3D-Systems Packaging Research  
Center

*[www.prc.gatech.edu](http://www.prc.gatech.edu)*

Atlanta, Georgia  
July 21, 2010

# Topics of Discussion

- Introduction - Prof. Rao R. Tummala
  - Purpose of Webinar
  - Why EMAP?
  - What is EMAP?
- Program Details - Mr. Nitesh Kumbhat (Program Manager)
  - Objectives
  - Comparison with Other Technologies
  - Recent Accomplishments
  - Research Tasks and Deliverables
- Execution Strategy - Mr. Nitesh Kumbhat
  - Uniqueness of Georgia Tech-Packaging Research Center
  - Membership Options and Costs
  - Next Step for Companies and for Georgia Tech

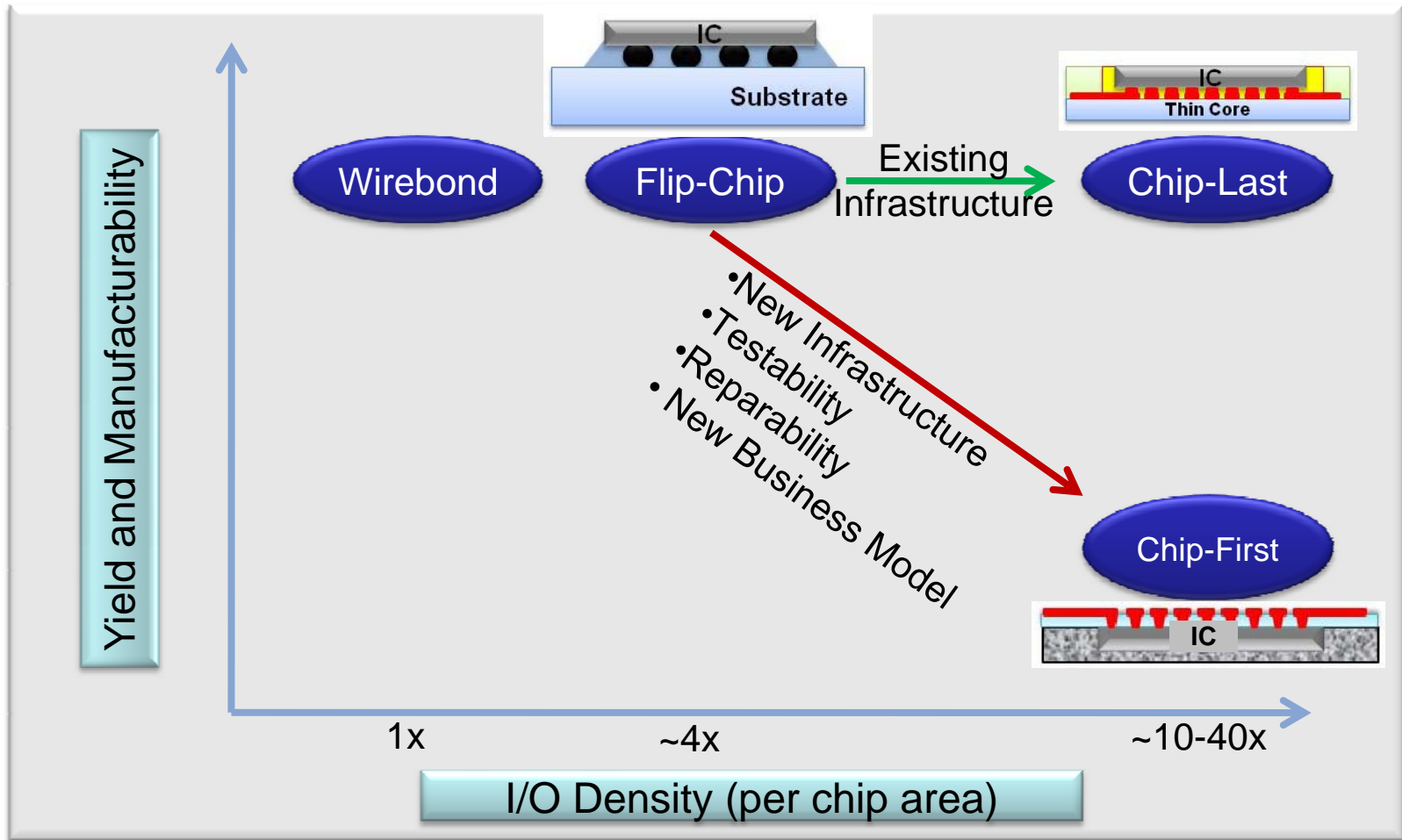


# Purpose of Webinar

- Invite Global Electronic Companies to Join GT PRC Consortium either as “Full Member” with IP rights or as “Supply Chain Member” to supply EMAP materials, tools, substrates, packages or modules:
  - For strategic technology
  - To leverage company funding by 10X
  - Utilize Industry-centric and proven team



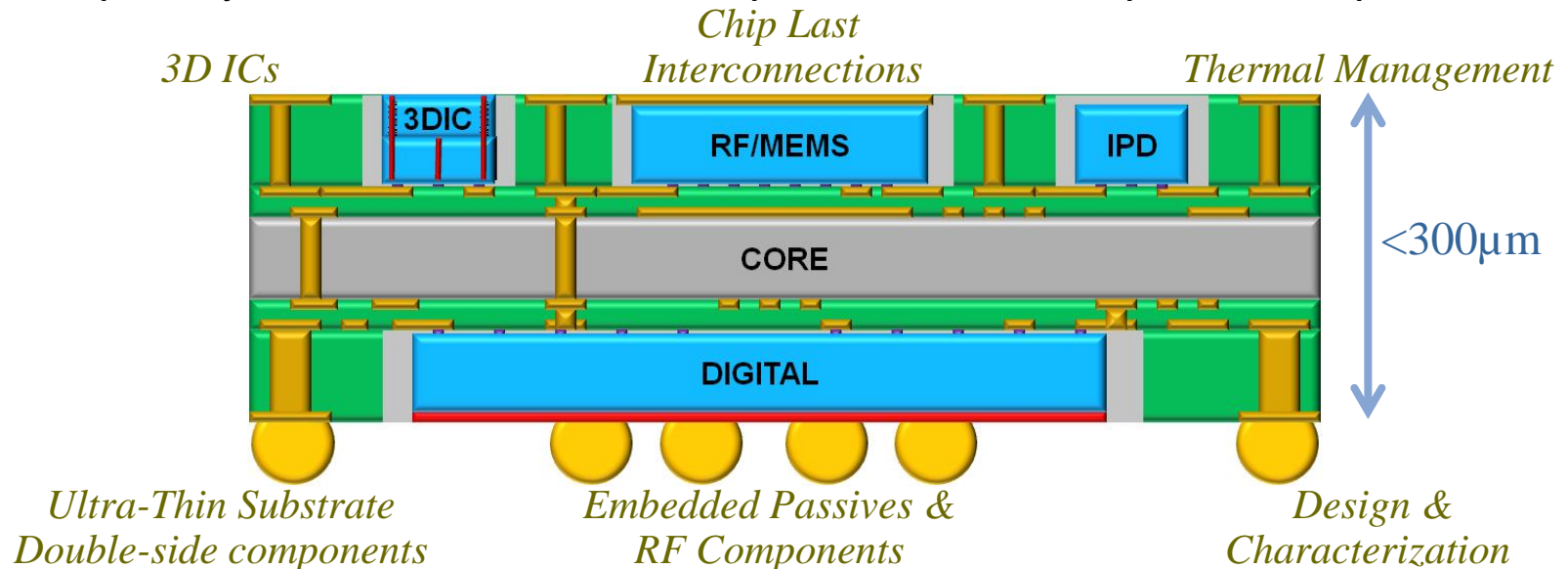
# Why EMAP?



# What is EMAP?

EMAP – Embedded MEMS, Actives and Passives

1. 5x smaller form-factor at module level for 1-110 GHz
2. Testability and repairability, leading to high yield
3. ULK- friendly and heterogeneous IC integration (MEMS, Analog, RF)
4. Compatibility with existing manufacturing infrastructure
5. 10x improvement in I/O density
6. Capability for Thin film embedded passives, MEMS, power components



# PHASE 2 PROGRAM DETAILS – MR. NITESH KUMBHAT

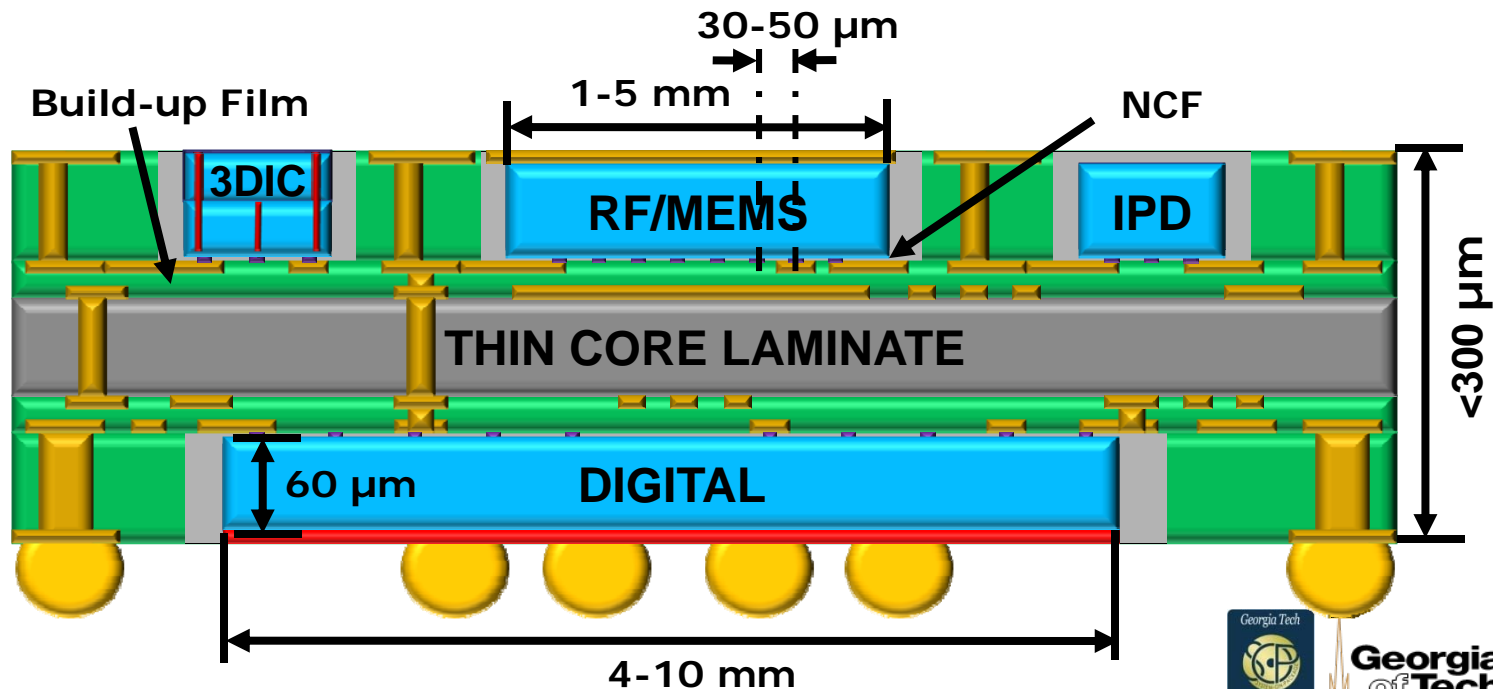


# Chip-Last EMAP Objectives

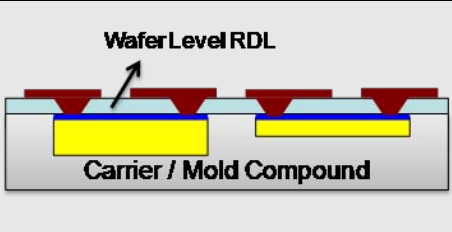
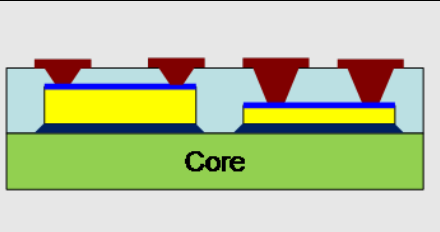
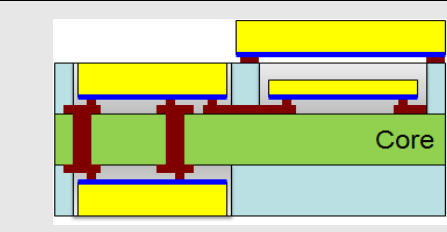
- Ultra-Thin Organic Modules with embedded actives and passives
  - Thinnest form factor (<0.5mm module height)
  - Finest pitch (30um pitch Chip-Last interconnects)
  - Highest Q embedded passives
  - Stable to 110 GHz and in high humidity
  - Heterogenous integration
    - Digital – High I/Os
    - Analog/RF – High precision embedded C and L
    - MEMS – Cavities
  - Manufacturing and supply chain

# Chip-Last Embedded Actives & Passives

- Heterogeneous, mixed-signal integration of Si, GaAs, IPD, MEMS devices
- Low-cost, manufacturing compatible processes
- Dedicated supply chain partners embedded in R&D program to commercialize EMAP technologies
- Functional RF & Digital module demonstration in 2010-2011



# EMAP Chip-Last Comparison with Other Approaches

	Chip-First Wafer Level Fanout	Chip-First Embedded IC in Substrate	Chip-Last Embedded IC in Substrate
Schematic			
Substrate Yield Concern	ICs committed prior to substrate process	ICs committed prior to substrate process	Substrate can be tested before committing ICs
Supply Chain Flow	<b>New Infrastructure Needed</b>	<b>Substrate → Assembly → Substrate</b>	<b>Substrate → Assembly</b>
IC Placement	<b>Precision Placement on Large Panel</b>	<b>Precision Placement on Large Panel</b>	<b>Precision Placement on Standard Strip Sizes</b>
Panel/Wafer Size	<b>Limited</b> Due to Dimensional Stability and Precise Lithography Need		<b>Not Limited</b> Due to Post-Placement of IC
Testability	Limited	Limited	Flexible Test Options
MEMS Integration	<b>Complex</b>	<b>Complex</b>	<b>Simple</b>

# Phase 2 Objectives

- Explore and demonstrate
  - Ultra-thin and high I/O organic substrate (10-15 $\mu$ m LW/S)
  - High-throughput cavities with <50 $\mu$ m chip clearance
  - 30 $\mu$ m pitch peripheral and 75-150 $\mu$ m pitch array interconnect
  - Technology demonstrator for benchmarking with eWLB
- Demonstrate functional module
  - Embedded ICs and embedded RF passives
  - RF Module for WLAN
  - Digital Mixed Signal Module with 250-500 I/Os

# Phase 1 Results: Ultra-Thin Low Loss Substrate & Fine Pitch Cu-to-Cu Interconnections

## 1-110 GHz Organic Substrate

Thin Core (100 $\mu$ m)  
Thin Build-up Film (20 $\mu$ m)

Low Dk & Df stable to 110GHz

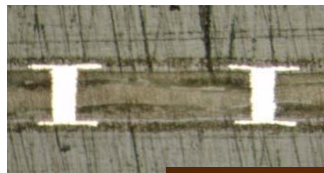
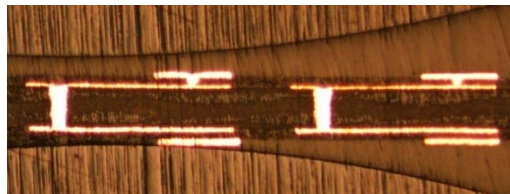
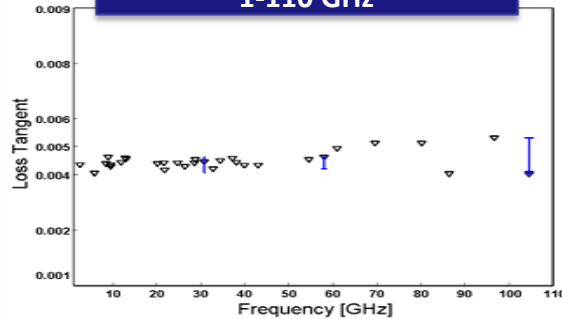
FR-4 Process Compatible

10 $\mu$ m Line/Space  
25 $\mu$ m Filled Blind Microvia  
30 $\mu$ m Filled TPV

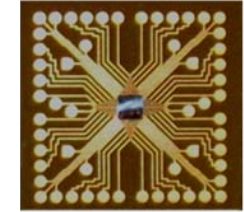
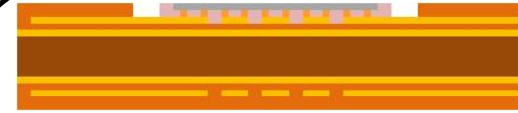
2000 cycles PASS

Loss Tangent 0.003 – 0.005

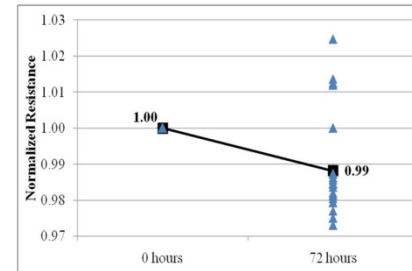
1-110 GHz



## Interconnections

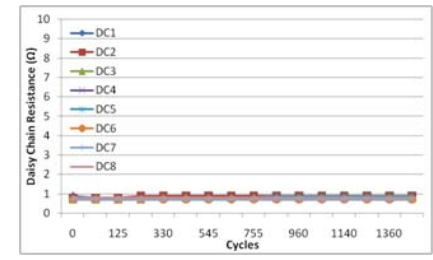
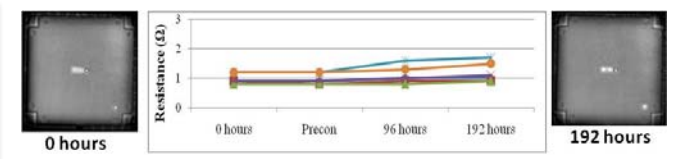


Cu Bump @ 30-50 $\mu$ m Pitch  
Adhesive Bonding @180 $^{\circ}$ C  
3 x 3 mm<sup>2</sup> and 7 x 7 mm<sup>2</sup> ICs  
Thin (~55 $\mu$ m) IC



**PASSED**  
72 hrs HTS at 175 $^{\circ}$ C

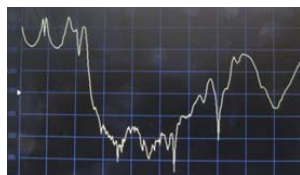
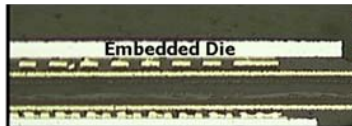
**PASSED**  
192 hrs HAST



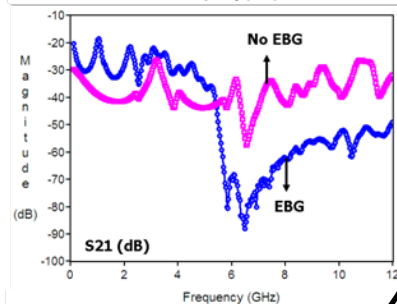
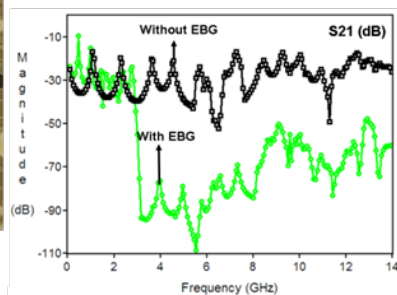
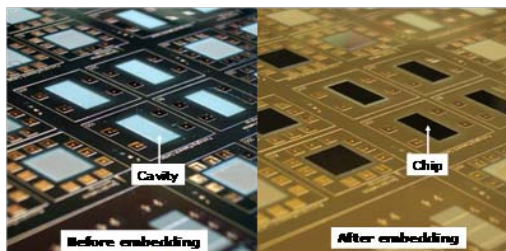
**PASSED**  
1400 Cycles  
-55 $^{\circ}$ C to 125 $^{\circ}$ C

# Phase 1 Results: Embedded Actives & High Q RF Passives

## Embedded Actives



Measured EBG Structures

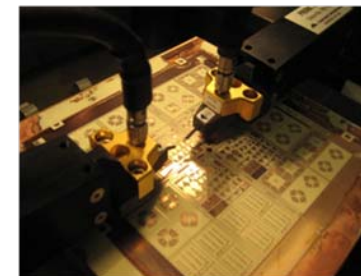
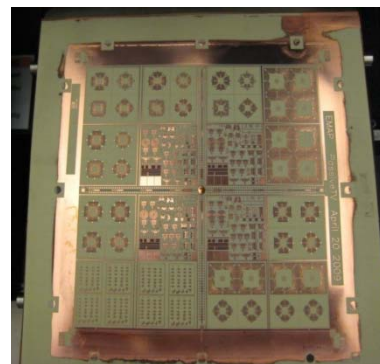


Passed 1000 Thermal Cycles (-55°C to 125°C) after MSL pre-con & 3x 260°C reflow @ 50µm I/O Pitch

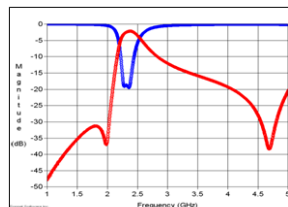
Highly Reliable

High isolation

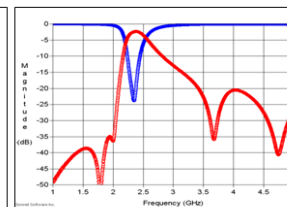
## Embedded Passives



Measured 2.5 GHz, 5 GHz Filters



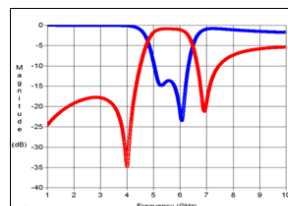
Insertion @2.38GHz: 2.2dB  
Attenuation @2.10GHz: 18.1dB  
Attenuation @4.71GHz: 39.1dB



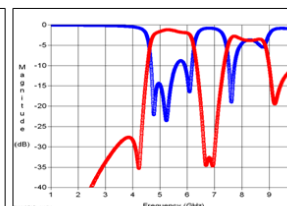
Insertion @2.38GHz: 2.3dB  
Attenuation @2.10GHz: 18.4dB  
Attenuation @4.74GHz: 40.6dB



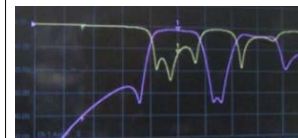
Volume < 1.2mm<sup>3</sup>



Insertion @5.4GHz: 0.9dB  
Attenuation @4.0GHz: 34.5dB  
Attenuation @7.0GHz: 21.2dB



Insertion @5.4GHz: 1.2dB  
Attenuation @4.2GHz: 35.1dB  
Attenuation @7.0GHz: 31.7dB

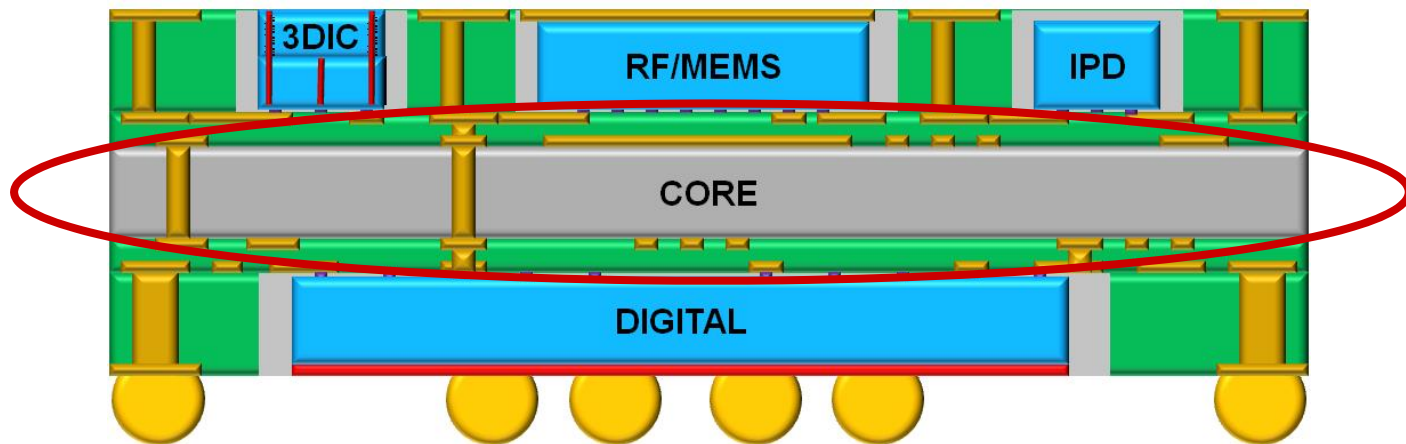


Volume < 0.6mm<sup>3</sup>

Low insertion loss and high attenuation

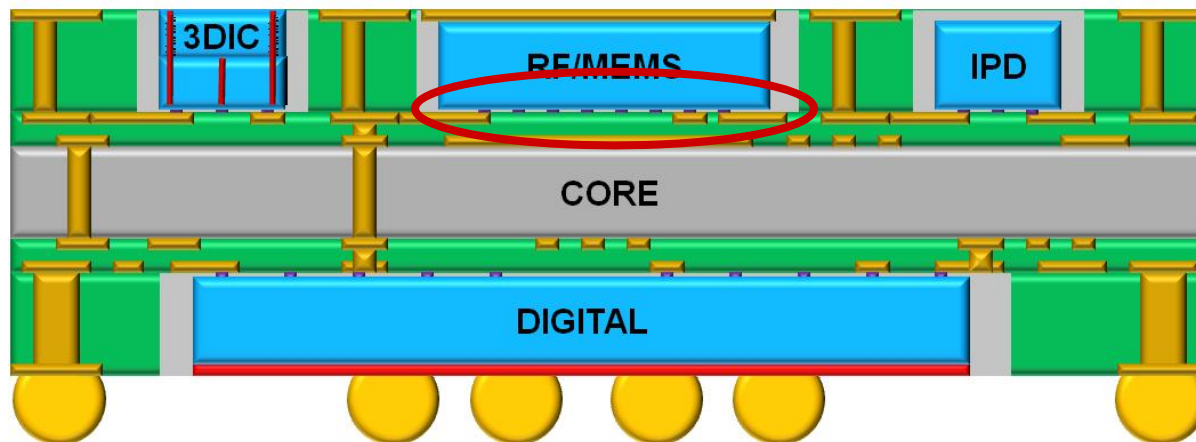
# EMAP Phase 2 Research Task 1

- Task 1: Halogen Free Substrate and Cavity
  - 1.1- Lower cost cavities in build-up substrate (4-6 metal layers)
  - 1.2- Two metal layer substrate with cavities



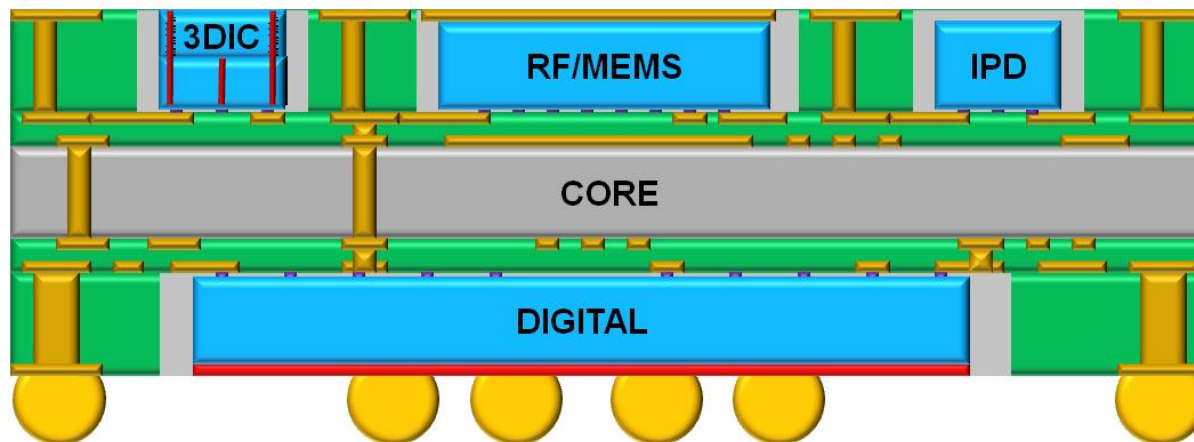
# EMAP Phase 2 Research Task 2

- Task 2: Interconnections
  - 2.1- Adhesive based bonding for ultra-fine pitch (30-100 $\mu\text{m}$ )
  - 2.2- Metallurgical bonding (80-150 $\mu\text{m}$  pitch)



# EMAP Phase 2 Research Task 3

- Task 3: Integration and Demonstration
  - 3.1- Digital and RF Functional Module
    - Technology comparison with eWLB
  - 3.2- Advanced EMAP Process Test Vehicle
  - Supply chain involvement



# EMAP Phase 2 Deliverables

- Fundamental Technologies
  - Ultra-thin and high I/O organic substrate (10-15 $\mu$ m LW/S)
  - High-throughput cavities with <50 $\mu$ m chip clearance
  - 30 $\mu$ m pitch peripheral and 75-150 $\mu$ m pitch array interconnect
- Demonstrators
  - Functional Module Demonstrators
    - WLAN Module - Embedded ICs and embedded RF passives
      - 2.4 GHz LNA, PA, Switch (all GaAs devices)
      - Microcontroller Mixed Signal IC with 250-500 I/Os
  - Technology Demonstrators
    - Full top surface availability for component placement and stacking
    - Two metal layer ultra-thin substrate (100 $\mu$ m) with embedded thin ICs
- Technology transfer to industry via supply chain partnerships



# EMAP 2 Team

- Center Director: Prof. Rao R Tummala
- Research Director: Dr. Venky Sundaram
- Program manager: Mr. Nitesh Kumbhat
- Substrate and Cavity Team: Dr. Fuhan Liu, Mr. Hunter Chan, Mr. Jason Bishop
  - Graduate Students: Mr. Vivek Sridharan, Mr. Felix Bergs
- Interconnection Team: Prof. C. P. Wong, Dr. Raj Pulugurtha, Dr. Jack Moon, Mr. Nitesh Kumbhat
  - Graduate Students: Mr. Abhishek Choudhury, Mr. Rongwei Zhang, Mr. Ganesh Hariharan
- Design Team: Prof. Sung Kyu Lim, Prof. Madhavan Swaminathan
  - Graduate Students: Mr. Gokul Kumar, Ms. Nithya Sankaran, Mr. Vivek Sridharan, Mr. Eddy Hwang
- Industry Liaison and Contracts: Mr. Dean Sutter



# EMAP Phase I & Phase II Companies

## Packaging Companies

AT&S  
 Endicott Interconnect  
 Ibsiden  
 Amkor\*  
 Wuerth Electronics\*

## OEMs / System Providers

Bosch  
 Draper Labs  
 Sameer

## Semiconductor and Component Makers

Epcos  
 Infineon  
 Intel  
 TI  
 Qualcomm  
 NXP  
 ST Microelectronics\*  
 National Semiconductor\*  
 TSMC\*  
 Triquint Semiconductor

## Tool, Process and Material Suppliers

Atotech  
 Brewer Science  
 Disco  
 DuPont  
 Mitsubishi Gas Chem.  
 Oak-Mitsui  
 Rogers  
 Sony Chemical  
 Starfire Systems  
 Siemens\*  
 Zeon Chemicals

Full Member  
 Supply Chain Member  
 \*Interested

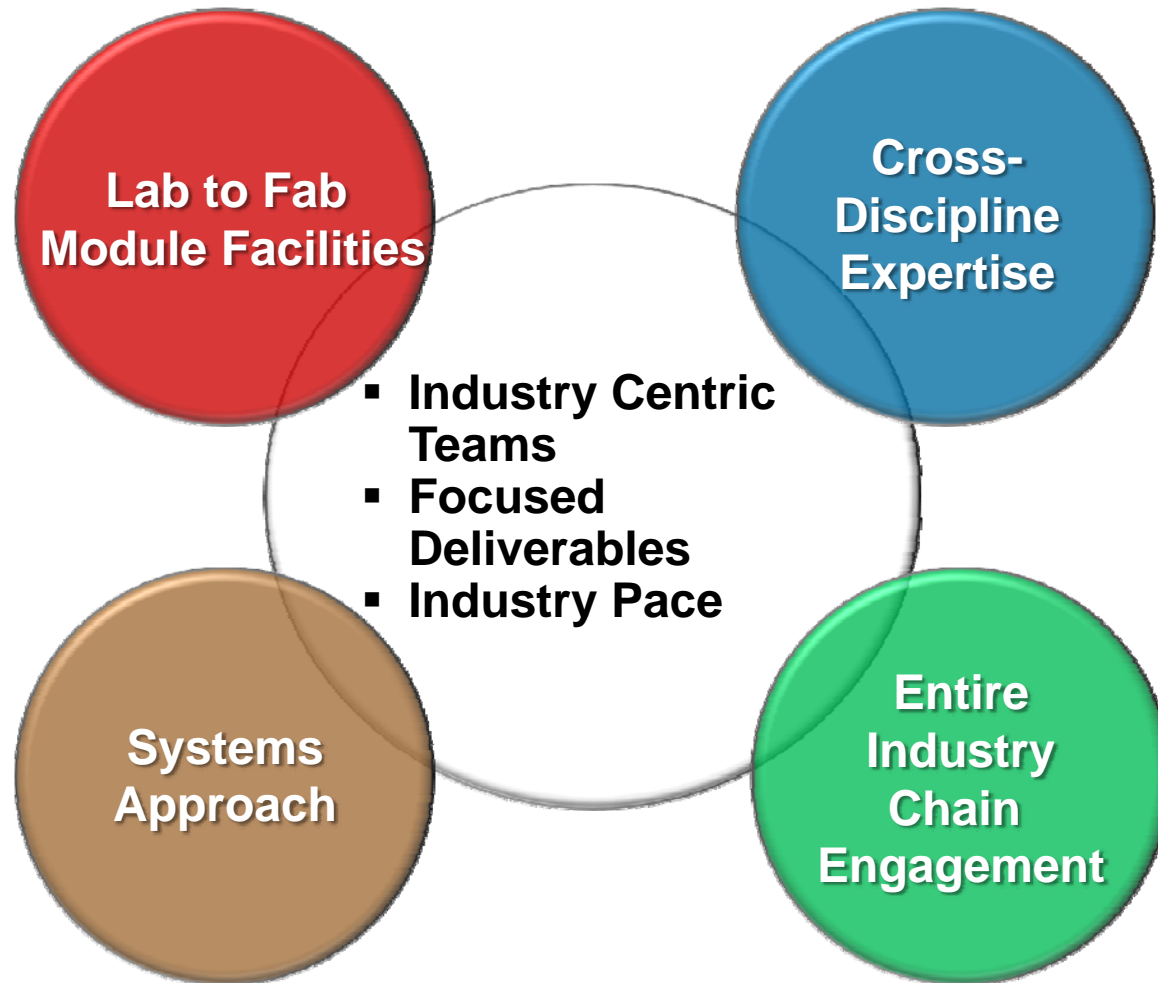


Georgia Institute of Technology



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# Uniqueness of 3D Microsystems Packaging Research Center



# Consortia Membership Benefits

Benefit	Full Member	Supply Chain
• Annual Membership Cost	\$100k	\$25K
• Program/Project Mentor	Yes	No
• Program/Project Steering	Yes	No
• I/P Rights – N.E.R.F License	Yes	No
• I/P Test Vehicle Rights/Info	Yes/Yes	No/Yes
• Meeting Participation	Yes	Yes
• Reports	Yes	Limited
• Materials/Equipment in Program	Yes	Yes
• Engineer-on-Campus	Yes	Yes “In kind” Related
• Leveraging of GT Know How	Yes	Yes
• Leveraging of Membership \$	Yes	Yes



# Next Step for Companies

- Phase 1 launched March 2007
- Phase 2 launched June 2010
- Asking companies to select one option
  - Full Member with IP rights
  - Supply Chain Partners
- Companies with high interest
  - Will receive White paper
  - Customized scope for full members
  - Next Face to Face Meeting at GT: November 8-9, 2010
- Contact Persons:
  - Mr. Nitesh Kumbhat: [nitesh@gatech.edu](mailto:nitesh@gatech.edu)
  - Mr. Dean Sutter: [dean.sutter@ece.gatech.edu](mailto:dean.sutter@ece.gatech.edu)
  - Prof. Rao R. Tummala: [rtummala@ece.gatech.edu](mailto:rtummala@ece.gatech.edu)





# EMAP II Webinar

*Thank you for joining us.  
For more information, contact:*

Mr. Nitesh Kumhbat,  
nitesh@gatech.edu,  
404-385-0730

*[www.prc.gatech.edu](http://www.prc.gatech.edu)*