Georgia Tech PRC
RESEARCH HIGHLIGHTS

"Pioneering Moore's Law for System Integration by System-on-Package (SOP) Concept"

Vol. 1 Issue 1
MARCH 2011

News

PRC Students Garner Accolades at ECTC 2010

Vivek Sridharan and Vijay Sukumaran, along with their advisor, Prof. Rao Tummala, were recognized for their outstanding research papers at the 60th Annual IEEE Electronic Components and Technology Conference (ECTC) in Las Vegas.

Vivek was given the Best of Session Award for "Design and Fabrication of Bandpass Filters in Glass Interposer with Through-Package-Vias (TPV)."

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Vijay won Intel's Best Student Paper Award for "Through-Package-Via Formation and Metallization of Glass Interposers."

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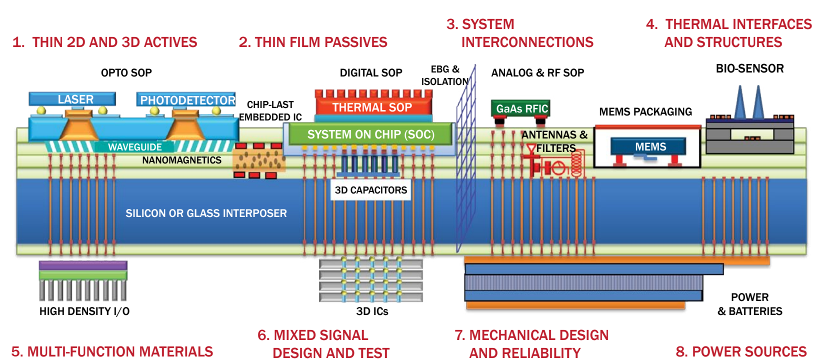
Georgia Tech PRC Announces Research Highlights in its Moore's Law for Systems Research

PRC Research Vision

In contrast to the well-known Moore's Law for transistor integration in ICs, which brought the industry to a $2T IT industry over the last 5 decades, and encompasses hardware, software, services and applications, Georgia Tech PRC believes that similar progress must be made in component integration to achieve highest functionality in smallest size at lowest cost at system level. This is referred to as Moore's Law for Systems. Such a vision is being pioneered by Georgia Tech PRC, leading to entire systems on a little package (SOP). This vision, depicted below, includes eight core technologies such as 1) thin film passives, 2) ultra-thin actives, 3) system interconnections, 4) thermal interfaces and structures, 5) nanoscale materials, 6) mixed signal design and test, 7) mechanical design and reliability, and 8) power sources.

Today, the PRC involves about 20 academic and research faculty and about 100 grad students In performing leading-edge device and systems packaging R&D in eight core research areas. Currently, the PRC is collaborating with about 70 companies from the US, Japan, Europe, Korea and India.

This issue features recent research highlights at GT PRC in the core research areas.



UPCOMING
Events

March 23
Learn how to connect with global packaging companies, universities, professional organizations and packaging industry publications at the UnITE™ PAC webinar.
dean.sutter@prc.gatech.edu
www.unite.globalgtprc.org

IN THIS ISSUE
Articles

U P C O M I N G
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March 30
Discover how GT PRC proposes to address fundamental material, process and manufacturing challenges in passive components, leading to 10-100X improvements in volumetric efficiency and component properties with a novel and unique set of organic, silicon or glass package-compatible thin film nanomaterials and processes, advanced tools and cleanroom facilities at the TPC Informational Webinar.
raj.pulugurtha@prc.gatech.edu
www.prc.gatech.edu

April 20
Learn how to connect with global packaging companies, universities, professional organizations and packaging industry publications at the UnITE™ PAC webinar.
dean.sutter@prc.gatech.edu
www.unite.globalgtprc.org

April 27
Discover how GT PRC proposes to address fundamental material, process and manufacturing challenges in passive components, leading to 10-100X improvements in volumetric efficiency and component properties with a novel and unique set of organic, silicon or glass package-compatible thin film nanomaterials and processes, advanced tools and cleanroom facilities at the TPC Informational Webinar.
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May 24 - 27
GT PRC hosts Consortia members for the 2011 IAB. This annual event features updates on research and industry programs for the EMAP, SiGI, TPC and UnITE™ PAC.
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May 25
PRC's two newest Consortias TPC and UnITE™ PAC will hold an Open Door Sessions on GT's campus during the 2011 IAB.
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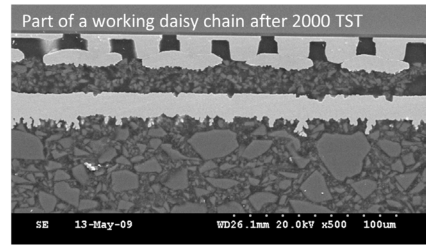
Interconnections

Highly-reliable, Low-temperature, Cu-Cu Interconnections with 5-10X Smaller I/O Pitch than Flip-Chip

Wirebonded interconnections have led to flip-chip in 1990s and more recently to copper bump or pillar interconnections. But these are still too bulky for ultra-miniaturized consumer electronics with their area array pitch of about 100-150µm. Chip-embedding is being pioneered to improve the both the size and density of interconnections by directwiring to the BEO, with particular focus on so called chip-first or chip-middle approaches. While these new interconnection technologies greatly improve the density and size, they create business, manufacturing, infrastructure and economic challenges. Georgia Tech PRC has taken an entirely different approach to achieve the same ultra high-density interconnections that chip-first enables but without its challenges. This approach is referred to as chip-last embedding, patented by Georgia Tech, which results in a more manufacturable, highly reliable, ultra-high I/O density Cu-Cu interconnections at less than 200°C. This research has demonstrated a unique and novel solution with excellent reliability results for ultra-fine pitch (~30µm) silicon IC-to-organic package interconnections using copper micro-bumps with nano-anisotropic conductive films and non-conductive films [1]. This research is being carried out in partnership with Bosch, Draper Labs, Epcos, Infineon, Intel, Namics, NXP, Qualcomm, SAMEER and TI.

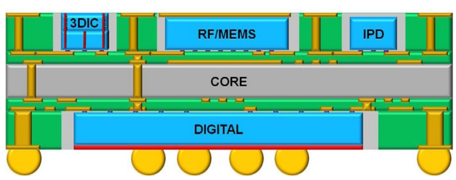


Cu microbump interconnect @ 30µm pitch and 10µm height

For additional information, please contact Nitesh Kumbhat at nitesh.kumbhat@prc.gatech.edu.

Ultra-Thin and Chip-Last Embedded Actives and Passive for Subsystem Functional RF Modules with Chip-First Benefits

GT-PRC has demonstrated a novel embedding approach using a chip-last embedding method and organic substrates with cavity, high yield and low cost, while retaining the electrical benefits of chip-first method [2]. Initial demonstrations were based on daisy chain test chips for process demonstration and reliability validation. The focus has recently moved to ultra-small form factor functional subsystem demonstration for dual-band WLAN modules with embedded filters and with both Si and GaAs ICs.



Embedded MEMS Actives and Passives (EMAP) Schematic

The total module thickness including embedded heterogeneous ICs and passives is targeted at <300µm. These modules are meant to serve as a functional demonstration of two fundamental technologies developed in GT PRC's Embedded MEMS, Actives and Passives (EMAP) program with main focus on: 1) advanced organic substrate technology with ultra-high I/O density, ultra-thin and low-loss; and 2) low-temperature Cu-Cu interconnections at ultra-fine pitch. Excellent RF performance has been recently measured in the first demonstration of these ultra-thin modules with embedded GaAs ICs and high Q filters in the same package.

This research is being carried out in partnership with AT&S, Atotech, Bosch, Brewer Science, Disco, Draper Labs, DuPont, Epcos, Endicott Interconnect Technology, Ibiden, Infineon, Intel, Maxim, Mitsubishi Gas Chemical, Namics, NXP, Oak Mitsui, Rogers Corp, Qualcomm, SAMEER, Sony Chemical, Starfire, Triquint Semiconductor, TI and Zeon Corp. Additional details can be found in the following publication: Fuhan Liu et al, "Chip-last embedded actives and passives in thin organic package for 1–110 GHz multi-band applications", Proceedings, Electronic Components and Technology Conference, 2010, pp. 758-763.

For additional information, please contact Nitesh Kumbhat at nitesh.kumbhat@prc.gatech.edu.

Silicon or Glass Interposer to Board SMT Interconnections

This research addresses a major fundamental reliability challenge as the semiconductor industry migrates from ICs to 3D ICs, both to achieve higher electrical performance and to integrate heterogeneous ICs. These 3D ICs with much smaller I/O pitch, about 5-10X smaller than flipchip, need an entirely new approach than the state-of-the-art organic packages to achieve 20-50µm pitch vs. current 150µm pitch, and at much lower cost. Silicon inter-

3D ICs need a new approach to achieve 20-50µm pitch vs. 150µm pitch at a much lower cost

poser packages are being developed widely to achieve these goals. However, silicon interposers present a major fundamental challenge due to the huge CTE mismatch between Si interposers of 3ppm/°C and 17ppm/°C for FR-4 board. To address this grand challenge, GT-PRC is exploring novel thin film, stress-relief interfaces with minimal electrical parasitics, adequate reworkability and advanced SMT interconnections. This interconnect solution is being developed to be compatible with standard SMT processes and tools, not requiring underfills. This research is being carried out in partnership with DuPont, Henkel, Intel, Qualcomm, Rogers, STMicroelectronics and Zeon Corp.

For additional information, please contact Nitesh Kumbhat at nitesh.kumbhat@prc.gatech.edu.

Power and RF

Nanomagnetics for Miniaturized Antennas

Antenna size is one of the biggest barriers to RF systems miniaturization. Integration of antennas with today's materials leads to bulky designs because antennas radiate effectively only when their size becomes an appreciable fraction of the wavelength. Embedded thin and miniaturized antennas with current approaches such as high-permittivity dielectrics or other advanced designs suffer from relatively narrow bandwidth due to substrate dielectric loss, mutual coupling with the substrate and surface wave propagation effects. Georgia Tech PRC has taken a fundamentally-new approach by exploring and developing a new class of nanoscale magneto-dielectric materials with high permeability, high permittivity, and low loss, at high frequencies. This unique combination of properties can potentially lead to 5-10X reduction in size and improve bandwidth, while simultaneously increasing the radiation efficiency. With novel nanoscale magneto-dielectric structures and processes, the PRC recently demonstrated high permeability of 3-4 and loss of 0.03 at VHF and UHF frequencies and a permeability of 2 at GHz frequencies, combined with high permittivity of 5-7.

For additional information, please contact Dr. Raj Pulugurtha at raj.pulugurtha@prc.gatech.edu.

Embedded Ultra-High-Density Capacitors

Thin film capacitors with high capacitance density are highly desirable but pose major challenges in achieving thin form factor, high capacitance density, low leakage and high breakdown voltage. To address these limitations, Georgia Tech PRC has recently explored, demonstrated and developed a novel approach that can potentially achieve 100-500 µF/cm^2 and yet achieve process-compatibility with silicon devices and silicon or organic interposers. The approach combines high surface area such as nanoelectrodes with conformal dielectrics and processes that are silicon or organic package-compatible. The first proof-of-concept prototypes showed capacitance densities of 30-50µF/cm^2 with 30 V BDV deposited on 50µm thick silicon substrate. This technology is being extended to higher capacitance densities with further enhancements in surface area, conformal processes and with higher-permittivity dielectrics. The novelty of the approach can potentially transform today's millimeter size bulky capacitor components that are mounted on packages and boards to micron-thick thin film components embedded in the package or in between 3D stacks.

embedded ultra-high density capacitors can potentially transform bulky capacitor components to thin film components

For additional information, please contact Dr. Himani Sharma at himani.sharma@prc.gatech.edu.

Miniaturized RF Components by Means of Glass Interposers

Next generation embedded and 3D-IC packaging technologies need to be more functional by incorporating embedded RF passives in the package. Choice of materials for such packages therefore becomes highly critical. Glass interposer offers the potential to combine the best attributes of ceramic interposers for RF performance and silicon interposers for high I/Os, without the high cost of both, thus providing a better alternative. Georgia Tech PRC recently demonstrated bandpass filters in glass interposer with insertion losses lower than 1dB using through-package-vias for the first time [3] it was seen that performance of glass interposer closely matches the performance of the more expensive, high-resistivity silicon. Based on this research, Georgia Tech PRC recently demonstrated the lowest volume WLAN filters [4], with chip-last embedded actives and is currently integrating these embedded passives into functional LNA and PA modules, as part of Chip-Last Embedded Actives and Passives (EMAP) program.

glass interposer offers the potential to combine best attributes of ceramic without the high cost

UPCOMING

Events

May 31 - June 3
Georgia Tech PRC team will present more than 20 papers at the 61st IEEE ECTC in Orlando, Florida. Topics include research findings on Panel-Based Polycrystalline Silicon Interposer, Low-Cost Glass interposers, Copper-to-Copper Interconnections, Chip-Last Embedded ICs, Ultra-Miniaturized WLAN RF Receivers, Fine-Pitch Flip-Chip Interconnections.

May 31 - June 3
Visit Georgia Tech PRC in booth #324 at the 61st IEEE ECTC in Orlando, FL. One-on-one appointments can be made through Dean Sutter.
dean.sutter@prc.gatech.edu

July 12 - 14
Visit Georgia Tech PRC in booth 6281 North Hall / 3D IC Pavilion at Semicon West 2011 in San Francisco, CA. One-on-one appointments can be made through Dean Sutter.
dean.sutter@prc.gatech.edu

GT PRC

News Flash

India Awards Georgia Tech Professor Rao Tummala Its Most Prestigious India Semiconductor Association's Technovisionary Award

This award honors a global citizen of any nationality for outstanding contributions related to semiconductors and electronics. The award has been instituted to recognize and honor a visionary who has over the years made seminal contributions that have made a difference to the electronics ecosystem. The awardees' path-breaking contributions could be in academics, research, industry or public service in the Electronics Packaging Field. Prof. Tummala accepted this award at the Annual India Semiconductor Association (ISA) Conference in Bangalore, India.

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University Industry Technology Ecosystem for Packaging (UnITE™ PAC) Launched

A low-cost entry level membership in PRC where companies can connect with each other, academia and other organizations to share common problems, define needs, and develop synergistic approaches to resolve infrastructure needs while sharing information in an open domain environment advancing the state-of-the-art of packaging, marketing their latest technologies and connect with students for internships and employment.

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www.unite.globalgtprc.org

Thin Film Passive Components (TPC) Consortium Launched

The Georgia Tech Packaging Research Center invites companies to join its new Global Industry R&D Consortium in Thin Film Passive Components (TPC) for analog, digital, power and RF functions in smart mobile electronics and implantable bio-electronic systems. The focus of the consortium will be: a) micro and nanoscale high-density and low-loss capacitors and inductors as surface thin film passives on silicon or glass with Through-Package Vias (TPVs) b) digital and RF passives as thin film Integrated Passive Devices (IPDs) with highpermittivity and permeability dielectrics and noise isolation structures. These thin IPDs can then be embedded into the package to realize total system miniaturization with improved performance.

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www.prc.gatech.edu/partnership/TPC

13 PRC Students to Present at 61st IEEE ECTC

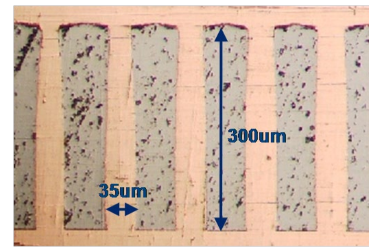
All PRC Students were accepted to present their research findings at this year's IEEE Electronic Components and Technology Conference in Lake Buena Vista, Florida this coming June. Research topics include:

For additional information, please contact Nitesh.Kumbhat at nitesh.kumbhat@prc.gatech.edu.

Silicon, Glass and Organic Substrates, Interposers and Packages

Modeling and Characterization of TSV Reliability

Through-Silicon-Via (TSV) technology is migrating from R&D into manufacturing for early 3D IC applications. However, two major concerns remain with TSV: cost and thermo-mechanical reliability. GT-PRC has been exploring a novel double-side TSV process to significantly reduce the cost of TSV fabrication through an SRC-funded research project whereby Silicon wafers are initially thinned down to 250-300μm thickness, followed by through via formation by DRIE process. All further process steps including oxide liner, barrier metals, and copper plating are performed in a double-side manner, without the use of any carrier or handling wafers. High speed electroplating processes are developed in partnership with Atotech for via fill and are analyzed for void formation and the effect of voids. In these studies, the TSV reliability has been modeled and is being assessed through thermal cycling tests. These studies led to 30-60μm diameter TSVs in 280μm thick CMOS-grade Si wafers using low-cost processes. This research is in collaboration with PRC faculty member Prof. Suresh Sitaraman in Mechanical Engineering [5].

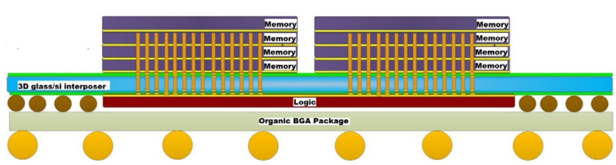


High aspect ratio TSV by a novel double side fabrication

For additional information, please contact Dr. Venky Sundaram, venky.sundaram@prc.gatech.edu or Qiao Chen at qiaochen198411@gatech.edu.

Glass and Silicon Interposers for High-Bandwidth Smart Mobile Applications as an Alternative to 3D ICs

Future generations of smart mobile systems must be capable of 3D graphics, HD displays and multimedia games. These systems, therefore, must be higher in bandwidth performance, and perform multiple tasks without an increase in size or power and at lower cost than today's systems. In addition, standardized interfaces that allow for the use of different devices and packages from suppliers are important. Current packaging approaches such as SIP, POP and F2F cannot be extended to achieve these goals, and TSV-based 3D ICs are being actively pursued worldwide. The GT PRC proposes an alternative approach to achieve high bandwidth at lower power and cost, without any disruption in wafer fabs for TSV fabrication in the logic chips. Georgia Tech PRC proposes to achieve high bandwidth by double-side interconnections, logic on one side and the memory stacks on the other side of ultra-thin glass or silicon interposers, with ultra-high I/O density and shortest interconnection length. This approach provides very large number of very short interconnections between logic and memory – the two fundamental parameters that drive bandwidth. The claimed benefits of 3D ICs can be harnessed without complicating the design and fabrication of the logic chip with TSVs. In addition, power delivery, electrical testability, reliability and system integration with multiple dies, become easier due to the nature of such a configuration. Initial modeling shows that even at low-frequency operation, high bandwidth rate, greater than 12.8GB/s can be easily obtained between logic and memory dies through short TPVs in glass interposers. This research is in collaboration with PRC faculty member, Prof. Sung Kyu Lim in Electrical and computer Engineering [6].

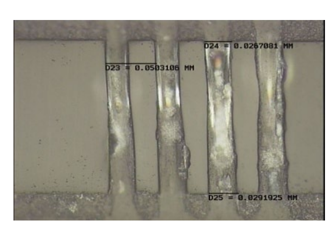


Interposer-based aproach to bandwidth

For additional information, please contact Gokul Kumar at gokul.kumar@gatech.edu.

First Demonstration of Glass Package with 50 Pitch in 175μm Glass

Packaging of 3D ICs requires an advanced interposer technology with high I/Os at small pitch and low cost. Organic interposers are limited in I/Os due to their poor dimensional stability for multilayer wiring, while silicon interposers are limited by their high cost. To address these limitations, GT-PRC is exploring an entirely different


Demonstration of 50μm pitch TPV

"Chip-Package Electrical Interaction in Organic Packages with Embedded Actives"

Nithya Sankaran
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Dr. Venky Sundaram
venky.sundaram@prc.gatech.edu

"Conformal Atomic Layer Deposition (ALD) of Alumina on High Surface-Area Porous Copper Electrodes to Achieve Ultra-High Capacitance Density on Silicon"

Dr. Himani Sharma
himani.sharma@prc.gatech.edu
Dr. Raj Pulugurtha
raj.pulugurtha@prc.gatech.edu

"Co-W as an Advanced Barrier for Intermetallics and Electromigration in Fine-Pitch Flipchip Interconnections"

Dibyajat Mishra
dmishra3@gatech.edu
Dr. Raj Pulugurtha
raj.pulugurtha@prc.gatech.edu

"Design and Demonstration of Low Cost, Panel-based Polycrystalline Silicon Interposer with Through-Package-Vias (TPVs)"

Mr. Qiao Chen
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Dr. Venky Sundaram
venky.sundaram@prc.gatech.edu

"Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through-Package-Vias"

Mr. Vijay Sukumaran
vsukumaran3@gatech.edu
Dr. Venky Sundaram
venky.sundaram@prc.gatech.edu

"High Density Electrical Interconnections in Liquid Crystal Polymer (LCP) Substrates for Retinal and Neural Prosthesis Applications"

Mr. Vijay Sukumaran
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Dr. Venky Sundaram
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"High Throughput and Fine Pitch Cu-Cu Interconnection Technology for Multichip Chip-Last Embedding"

Mr. Nitesh Kumbhat
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material and process system using low cost packaging approaches and glass as well silicon in panel form. Glass as an interposer material has several merits. It is of high electrical resistivity, available in thin and large panel sizes and infrastructure for handling such has been developed for LCD displays. It has two challenges, however: how to make small holes at low cost and its low thermal conductivity compared to silicon. The Georgia Tech PRC is pioneering a total system approach with particular focus on solving these two problems by fundamental design, modeling and simulations, novel dielectric, conductor and through-package-via materials and processes in panel form. An initial global industry consortium consisting of Asahi Glass, Atotech, Corning Glass, Dupont, Henkel, Life Bio Sciences, Maxim, Namics, Oracle, ST Micro, Qualcomm, Rogers, Zeon Corporation, and Shinko is in place while additional new members are being sought. As part of this Silicon and Glass Interposer (SiGI) industry consortium, the Georgia Tech team has already demonstrated through-via formation and metallization of vias at 50µm pitch in thin glass panels of 175µm thickness [7]. Further studies are underway to design and fabricate ultra-fine pitch and reliable TPVs in glass.

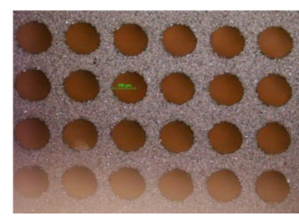
For additional information, please contact Vijay Sukumaran at vsukumaran3@gatech.edu or Dr. Venky Sundaram at venky.sundaram@prc.gatech.edu.

PRC Develops Low-cost Silicon Interposer with Fine Pitch Through-Package-Vias (TPV)

Silicon interposers, initially thought to be an intermediate step before full 3D IC integration are now considered a mainstream technology to replace organic packages for high I/Os and for packaging of ICs with ULK. While silicon interposers have already been demonstrated with small-pitch I/Os, it is becoming clear that wafer-based silicon interposers suffer from high cost that only high performance applications could afford. The focus of Georgia Tech PRC in silicon interposers is to demonstrate low cost interposers.

Such a low cost focus has five key elements:

1. Use of polycrystalline silicon, in contrast to single crystalline silicon with wafer-based approaches;
2. Large panel-based silicon in 700mm x 700mm size and without back-grinding or chemical-mechanical polishing to achieve 150-200µm thin cores, a factor of more than 10X in area over wafer-based silicon;
3. Laser ablation to form TPVs down to 10µm diameter without any debris;
4. Low-temperature and thicker polymer liner in contrast to the high temperature and thinner, oxide liner; and
5. Double-side processing using low-cost dry film polymers to act as dielectrics for RDL and all-wet metallization processes for conductors vs. BEOL for traditional Si interposers.



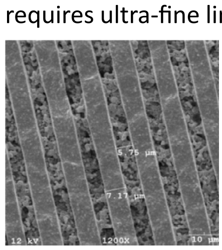
Top view of 200µm pitch TPVs in panel silicon

GT PRC has demonstrated all these low cost building-block technologies and will integrate and optimize them further in 2011.

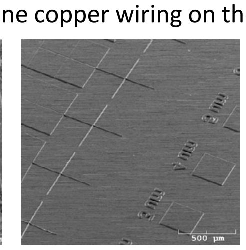
For additional information, please contact Dr. Venky Sundaram, venky.sundaram@prc.gatech.edu.

Low-cost 5µm RDL Technology

The semiconductor industry's transition to 3D ICs, has accelerated the need for I/O pitch reduction at package level. Fine pitch of 40-50µm in area array and 20-30µm in peripheral interconnect pitch requires ultra-fine line copper wiring on the package substrate or interposer. For example, if three lines per channel are required for routing a chip with 60µm pitch I/Os, the redistribution layer (RDL) has to have line width and spacing no larger than 5µm. If additional requirements such as flatness and low coefficient of thermal expansion are required, glass or silicon-based package technology is the best way, since they provide extremely high density wiring including fine pitch through holes and fine pitch copper traces. Georgia Tech PRC has been exploring low cost 5µm RDL technology in organic substrates [8-9] and more recently on thin and large silicon and glass panel-based substrates. Copper line width and spacing of 4µm to 6 µm was demonstrated using low cost photo resists, full- field i-line (365nm) UV exposure lithography, electroless copper plating



SEM image of plated 7µm Copper traces with 6µm spaces on organic substrate

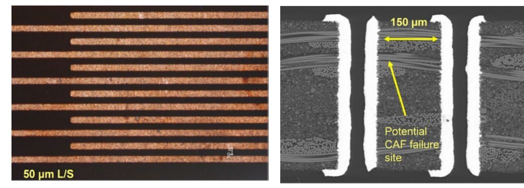


SEM image of photo resis with 2-5µm widths on silicon substrate for conductive seed layer and electrolytic copper plating. All these materials, processes, and tools are compatible with large panel substrates and PCB infrastructure.

For additional information, please contact Dr. Fuhan Liu at fliu@ece.gatech.edu.

Green Electronics and Reliability

The European Union's Restriction of Hazardous Substances (RoHS) regulations have limited the use of halogens and lead-based solders in electronic devices. This enables environmentally-safe recycling and prevents the release of toxic gases such as dioxins and furans into the environment, thus enabling "green" electronics. These requirements have led to the development of a new class of polymer-glass laminate materials with halogen-free flame retardants. At the same time, Moore's law and 3D ICs require high I/O organic substrates with fine pitch wiring and through-package-vias for achieving system miniaturization. These new requirements raise serious reliability concerns in surface and sub-surface insulation resistance loss with all the new halogen-free substrates. This research, in partnership with industry, investigates the reliability of ultra-fine pitch conductors (<50µm) and through-package-vias with fine pitch (< 250µm) in package substrates with halogen-free formulations, consistent with ITRS roadmap targets. Georgia Tech PRC is conducting accelerated reliability testing to investigate the surface (Surface insulation resistance) and sub-surface (Conductive anodic filament) reliability of fine pitch conductors and fine pitch through-package-vias [10]. Test patterns used for SIR test with 50µm line/spacing and SEM image of cross-section of a CAF test coupon with 100µm through-vias with 150µm spacing are shown in the figure above.



SIR test coupon with 50µm coper lines/spacing in halogen-free substrates (left) and CAF test coupon with through-vias 100µm with 150µm spacing in a halogen-free substrate (right)

There are additional reliability concerns for these new materials imposed by Pb-free interconnections requiring high temperature assembly processes. Therefore, reliability of Pb-free interconnections under highly accelerated stress and humidity conditions, high temperature storage and thermal cycling are also under investigation. This important research will enable ultra-fine pitch packaging and green electronics.

For additional information, please contact Koushik Ramachandran at koushik@gatech.edu.

Electrical Design of Silicon and Glass Interposers

3D ICs require interposers with I/O pitch down to 30µm and lithography ground rules for copper traces around 1-5µm. While several groups have identified glass as a better interposer material, Georgia Tech PRC (GT-PRC) has developed one of the most comprehensive, pioneering programs in exploring developing and designing glass as a low-cost and high I/O interposer. The electrical behavior of Through-Package-Vias (TPVs) in glass interposers was studied and compared with TSVs in silicon interposers, for the first time [11]. The effect of different TPV formation processes on the insertion loss and crosstalk was also studied by means of electromagnetic (EM) simulations [7]. Georgia Tech PRC has also performed electrical modeling, design, and characterization of glass interposers by focusing on parasitic extraction of TPVs in glass interposer by simulation and measurements and, modeling and simulation of the entire interconnection path through the glass interposer (from the BGA connection to the I/O circuit driver in the IC). The characterization of the panel-based glass and silicon interposers, along with the different interconnection elements (for e.g., TPV, re-distribution layer wiring, etc.) by design, fabrication, and measurement are underway as part of the SiGI industry consortium in partnership with 20 companies in the US, Japan, Europe and Korea.

GT-PRC has pioneered programs in glass as low-cost and high I/O interposer

For additional information, please contact Tapobrata Bandyopadhyay at tapobrata@gatech.edu.

Thermal Technologies

Novel Nanocomposite Plating Approach for Metal-based TIM

Thermal management has always been a grand challenge both for traditional microprocessor packages and for the emerging through-silicon-via-based 3D ICs with through-package-via-based silicon or glass interposers. Polymer composites have been the industry work-horse for thermal interface materials (TIM), although the majority of polymer TIMs have a bulk thermal conductivity

"Low cost, Chip-Last Embedded ICs in Thin Organic Cores"

Mr. Nitesh Kumbhat
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"Novel nanomagnetic materials for high-frequency RF Application"

Dr. Himani Sharma
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Dr. Raj Pulugurtha
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"Reliability of Ultra-Fine Pitch Halogen-Free Organic Substrates for Green Electronics"

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"Solution-Derived Electrodes and Dielectrics for Low-Cost and High-Capacitance Trench and Through-Silicon-Via (TSV) Capacitors"

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"Ultra-high I/O Density Glass/Silicon Interposers for High Bandwidth Smart Mobile Applications"

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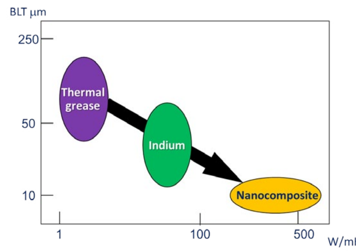
"Ultra-Miniaturized WLAN RF Receiver with Chip-Last GaAs Embedded Active"

Mr. Nitesh Kumbhat nitesh.kumbhat@prc.gatech.edu of less than 4-5 W/mK, even with the maximum loading of conductive fillers. Emerging metal-based TIM is also limited due to the high CTE mismatch between it and with either the IC or the heat spreader, resulting in high stresses. Georgia Tech PRC recently explored novel high conductivity tin and indium-based ceramic composite TIM bonding layers (50-100µm) using a co-electroplating technology. In this research, TIM layers were electroplated by modifying commercial solder plating chemistries to yield graphite-loaded solder nanocomposite films. The metal-graphite nanocomposite approach lowers the CTE to that of the heat-sink while enhancing the thermal conductivity by 1.5-2X compared to indium. The plating approach allows controlled thin film deposition with a scalable batch processes. Preliminary prototypes showed good adhesion strength even with 60-70% graphite loading in indium [12].



Trend to advanced TIM with nanoscale materials

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