Silicon and Glass Interposer (SiGI) Applications

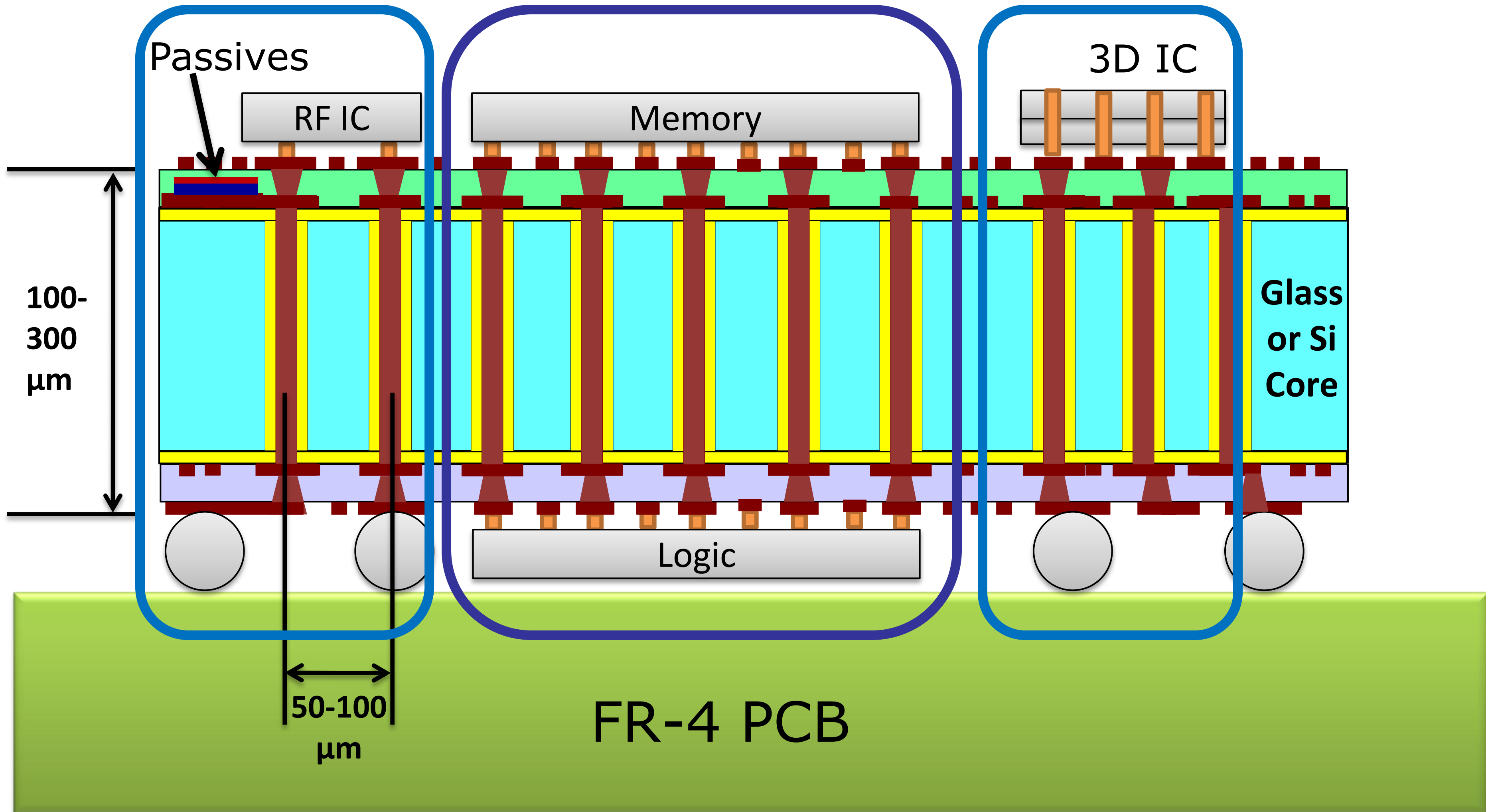
May 25, 2011

Atlanta, GA

Dr. Venky Sundaram

CONFIDENTIAL

Silicon and Glass Interposer (SiGI) Concept



Georgia Tech Packaging Research Center
Georgia Institute of Technology

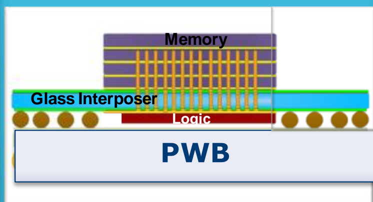
CONFIDENTIAL

SiGI Applications

Consumer Mobile

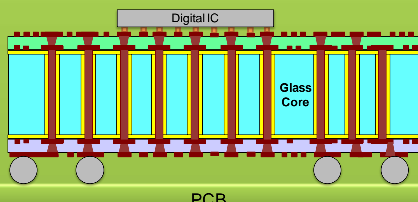
High Bandwidth Package

- Logic-memory Integration



Mixed Signal Package

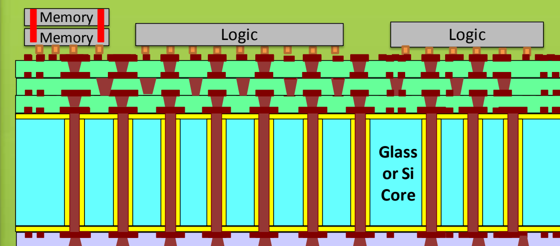
- Digital - 3DIC or ULK IC package
- RF
- Analog/MEMS package



High Performance

BGA Package or Interposer

- High I/O 3D-IC or ULK IC Package
- Multi-chip interposer for <32nm
- Logic-Memory High Data Rate



Package Size	7mm	10mm	20mm	50mm
Chip I/Os	1024	3000	5000	10000
Si/Glass Thickness	30µm	50µm	100µm	200µm
RDL L/S	15µm	10µm	5µm	1µm
TPV Pitch	20µm	60µm	100µm	200µm

SiGI Building Block Technologies

Packaging Research Center of Technology

CONFIDENTIAL

Research Targets: Consumer Mobile vs. High Performance

Parameter	SiGI Mobile		SiGI High Performance
	Mixed Signal	Logic-Memory	
Glass or Si Thickness	50-100µm	30-50µm	100-300µm
TPV Diameter TPV Pitch	30-60µm 60-100µm	5-20µm 10-50µm	30-100µm 100-200µm
RDL Layer Count	0+2+0 1+2+1	0+2+0 1+2+1	2+2+2 3+2+3
RDL Line & Space	7-15µm	3-5µm	3-5µm
RDL Blind Via Diameter	15-25µm	3-10µm	3-10µm
Chip Size	5-10mm	5-10mm	15-25mm
# of 1st Level I/Os	1000-4000	1024 (IC-IC)	10000
1st Level I/O Pitch	20-30µm Peripheral	20-50µm Multiple Rows	30-50µm Array
2nd Level I/O Pitch	300-400µm	300-400µm	800-1000µm
Package Body Size	7-15mm	10-15mm	40-60mm
Phase 1 Timeline	2010-2012	2011-2013	2011-2013

Georgia Institute of Technology

SiGI Mobile

Miniaturization and Low Profile Glass and Silicon Package

SiGI Mobile R&D Focus

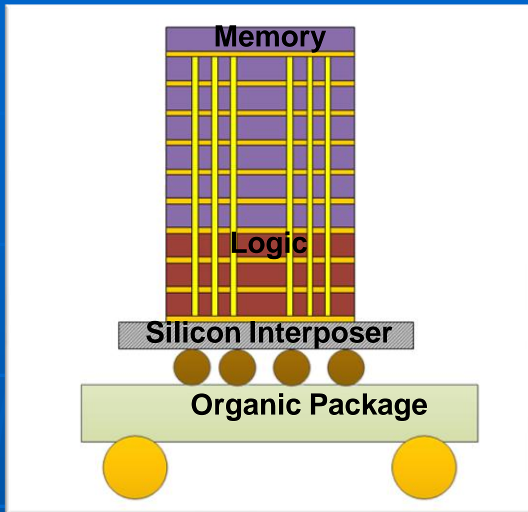
- Ultra-thin core (50-100um glass by draw process)
  - Fine pitch laser TPV (conformal or filled metallization)
- No build-up or one build-up layer on either side of two-metal layer core by semi-additive or subtractive process
- Fine Pitch BGA (300um) from Si or Glass Package to PWB
- Embedded actives and passives for DC-10GHz and beyond

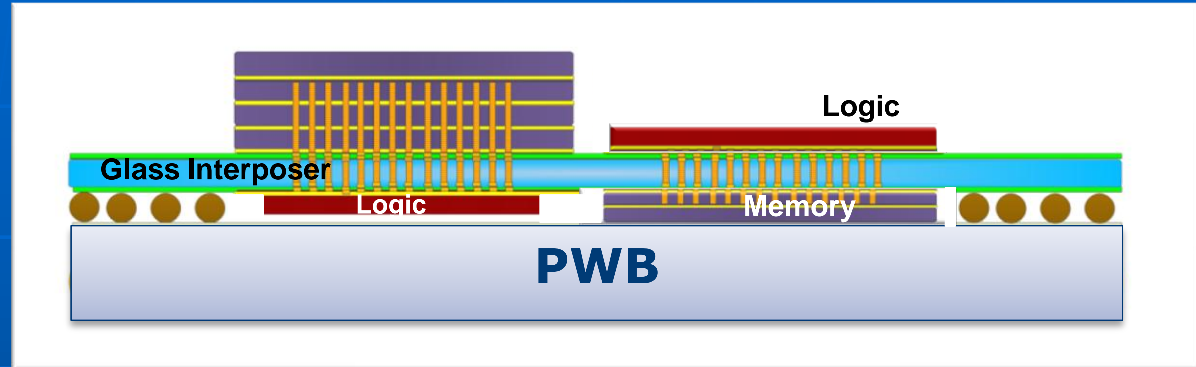
SiGI Bandwidth

High Bandwidth Ultra-Thin Glass Interposer
Without TSV in Logic

Georgia Tech Packaging Research Center
Georgia Institute of Technology

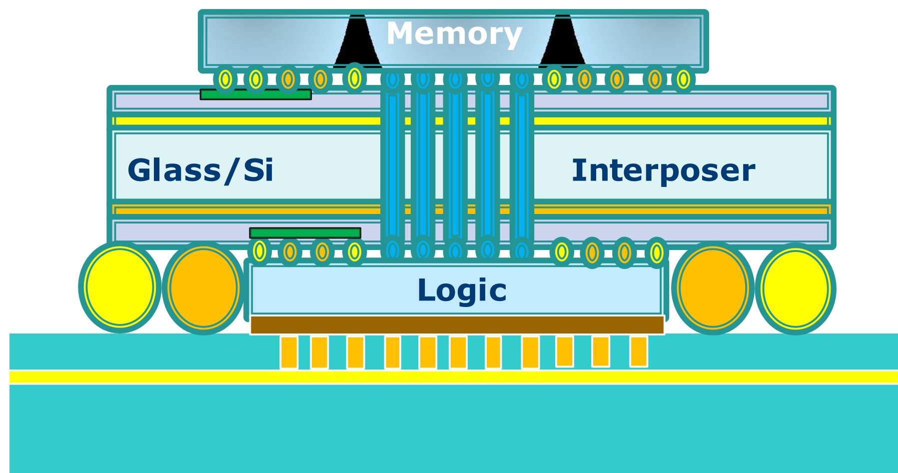
TSV-Die Stacking vs TPV-Glass Die Mounting



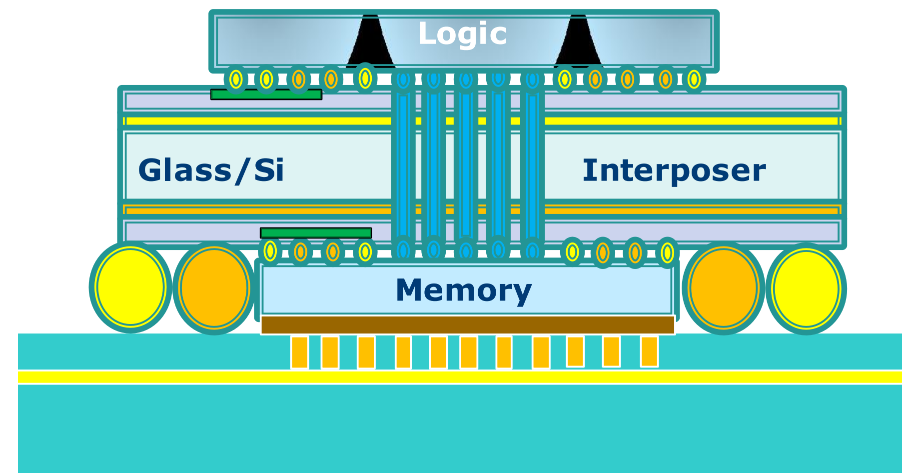


Parameter	TSV Die Stack	TPV Glass Interposer
Cost	Medium -> High	Lower
Bandwidth	High	High
Reliability	Med	High
Latency	Small	Med -> Small
Unit of Power/Bandwidth	Low	Low
Scalability	Low	High
Flexibility	Low	High
Heterogeneous	Low	High

SiGI for High Bandwidth Logic-Memory Interconnects



Lower Power Logic



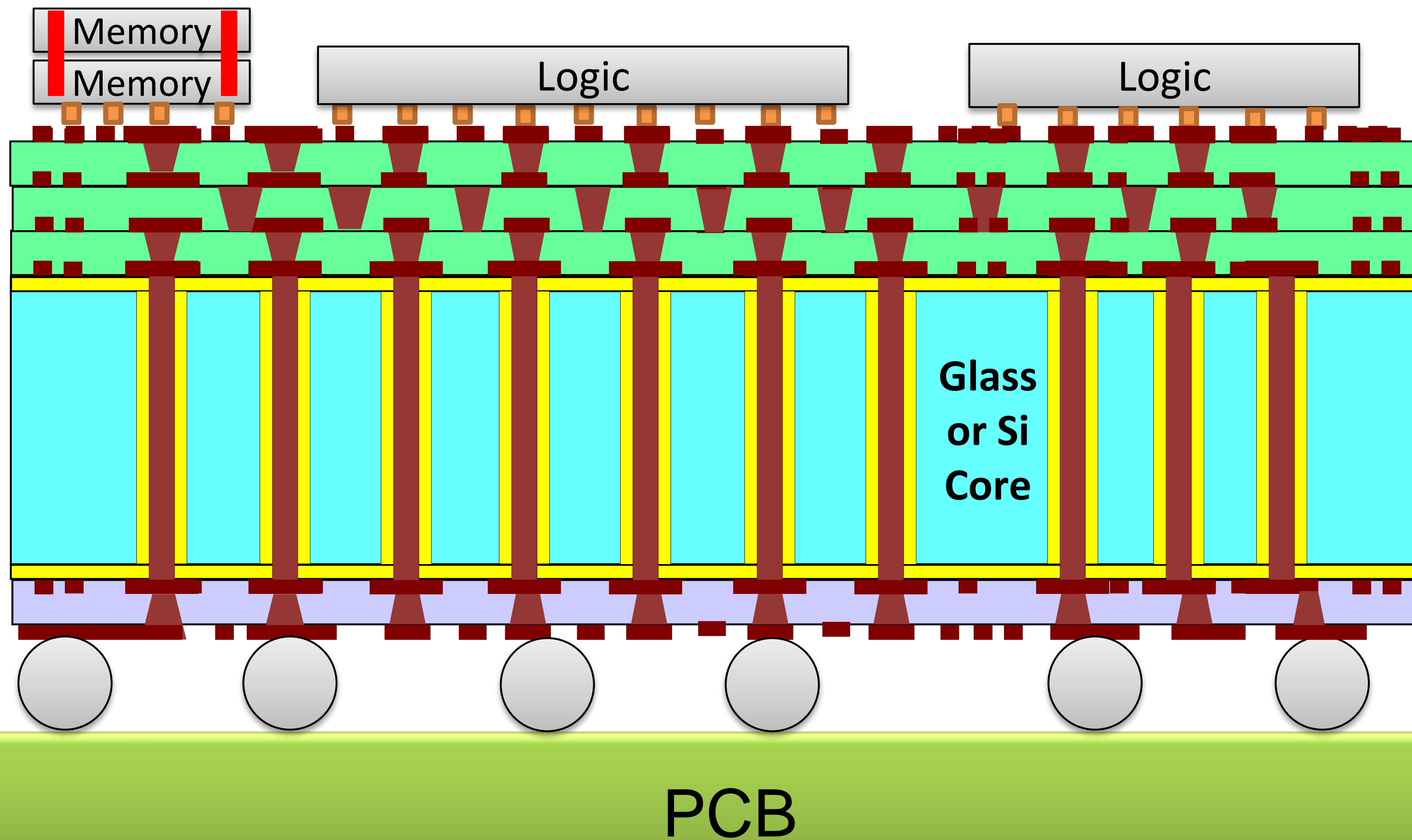
Higher Power Logic

- An alternate solution to TSVs in logic
- Enabled by ultra-thin glass with ultra-small and fine pitch TPVs
- Capability for High Bitrate using low-loss TPVs
- Better thermal and testability options

Georgia Tech Packaging Research Center
Georgia Institute of Technology

CONFIDENTIAL

SiGI Processor Package



Georgia Tech
PACKAGING RESEARCH CENTER
Georgia Institute of Technology

CONFIDENTIAL

SiGI Processor Package R&D Focus

- Thin low CTE core (100-200um silicon or glass panel)
  - Matched CTE for ULK integrity
- **2-3 build-up layers on both sides of core**
  - **<10um blind microvias**
  - **3-5um RDL lines beyond semi-additive process**
- **5000-10000 chip-to-interposer I/Os at 15-50um pitch**
  - **All Cu interconnect by low temperature bonding**
- Improved thermal dissipation in silicon or glass interposer
- **Embedded decoupling capacitors in interposer**
- **Power and signal integrity co-design of IC and interposer**

Georgia Tech Packaging Research Center
Georgia Institute of Technology