# Silicon Interposer Mechanical Design for Reliability

**Suresh K. Sitaraman, Ph.D.**
**Professor**
**The George W. Woodruff School of Mechanical Engineering**
**Georgia Institute of Technology**
**Atlanta, GA 30332-0405**
**Phone: 404-894-3405; FAX: 404-894-9342**
**email:suresh.sitaraman@me.gatech.edu**

**Collaborators: Dr. V. Sundaram, Prof. R. Tummala**
**Students: X. Liu, Q. Chen**

# Outline

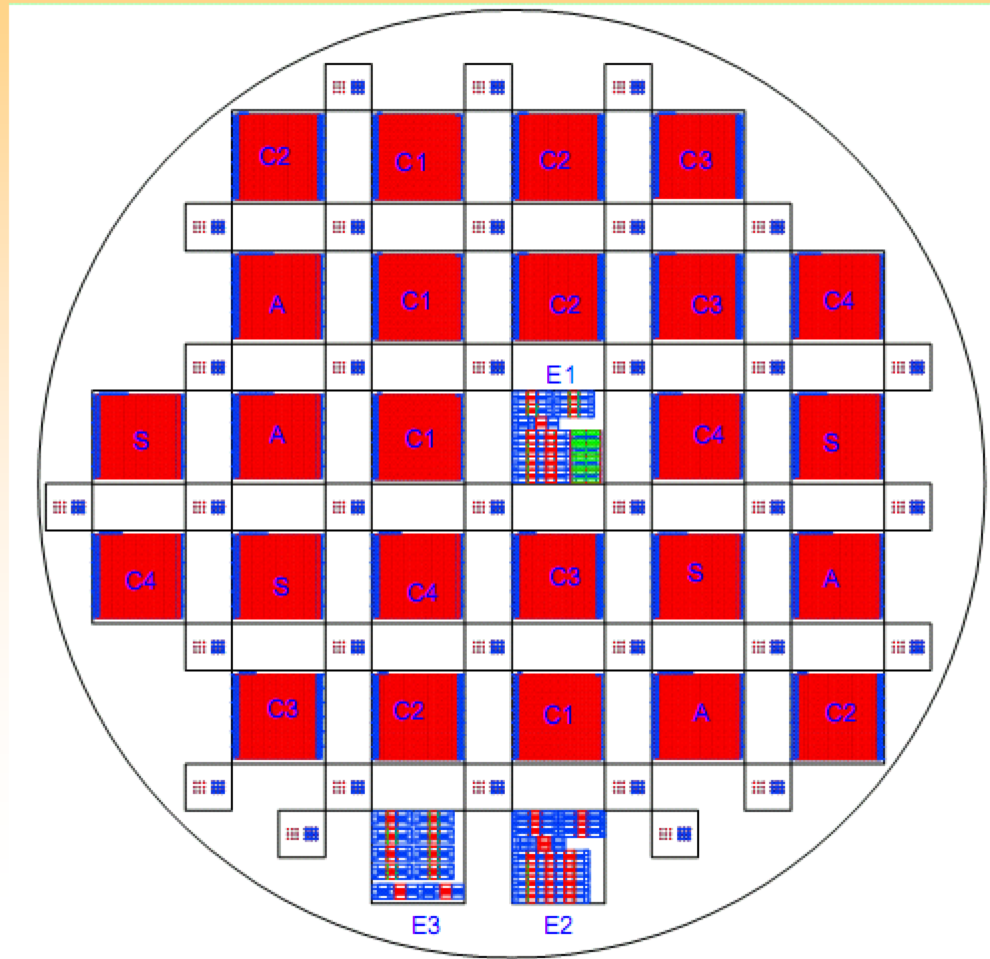
- Why TSV?
- TSV Fabrication
- TSV thermal shock test
- Thermo-Mechanical Reliability Modeling and Results
- Summary

# Motivation for 3D ICs with TSVs

- Motivation: Vertically integrate and connect semiconductor strata to combine similar or hybrid technologies to gain:
  - Reduced interconnect latency
  - Reduced interconnect power consumption
  - Increased bandwidth
  - Reduced form factor
  - Integration of differentiated technologies
  - Yield improvement (compared to SoC)

# Mask Layout

**28 Coupons per wafer**

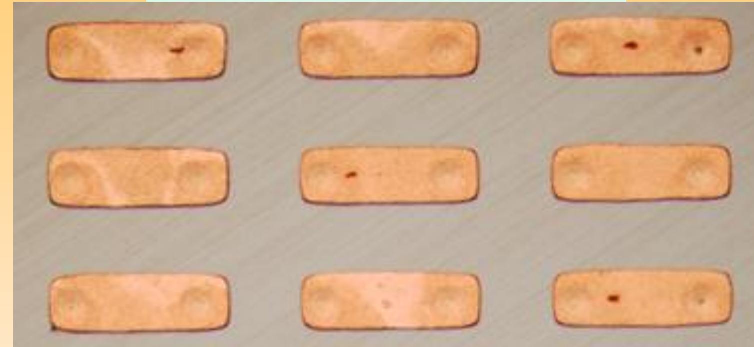


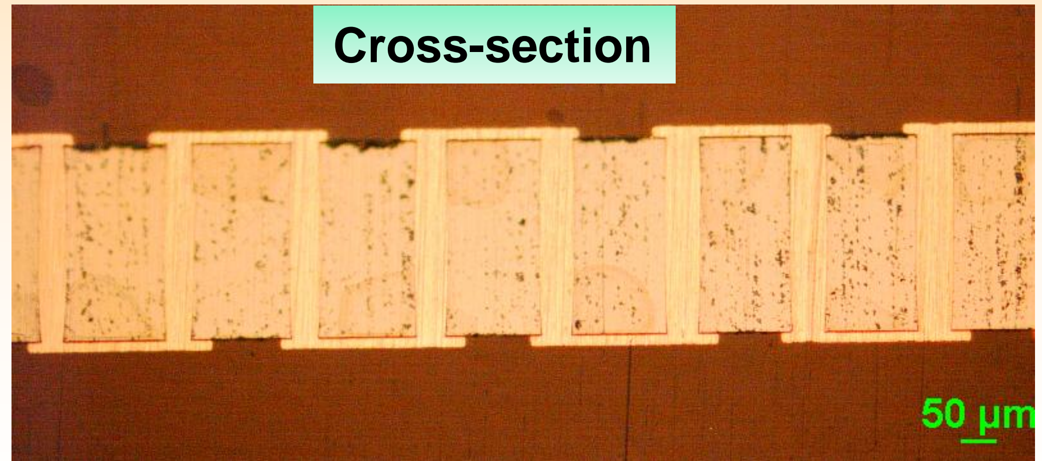
# TSV Fabrication and Reliability Analysis

- Lithography
- Via Etch (Through)
- Liner Deposition
- Barrier/Seed Plate
- Electroplating
- Copper Thinning
- Lithography
- Etch/Strip
- Planarization (optional)

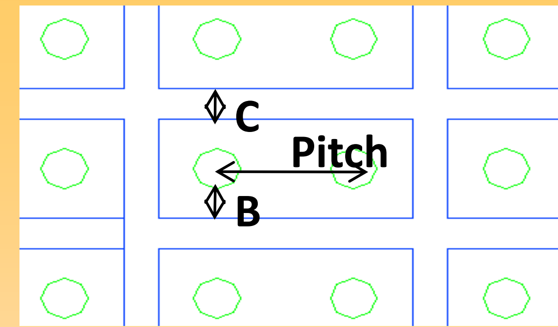
**Double Side TSV in Si**

Top view (Cu pads)





# TSV Daisy Chain Design




| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C2) | 40 | 30 | 30 | 130 |
| Circle (C3) | 40 | 30 | 55 | 155 |
| Circle (C4) | 65 | 30 | 30 | 155 |

Pitch Effect

Diameter Effect

| TSV | Side (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Square (S) | 57 | 30 | 38 | 155 |

| TSV | Inner Diameter (um) | Outer Diameter (um) | Gap (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|---|---|
| Annular (A) | 25 | 65 | 20 | 30 | 30 | 155 |

Shape Effect

# Thermal cycling test status (-40$^0$C to 125$^0$C)

- Samples have gone through 700 cycles thermal cycling test
- No failure occurs based on daisy chain measurement

# Simulation Outline

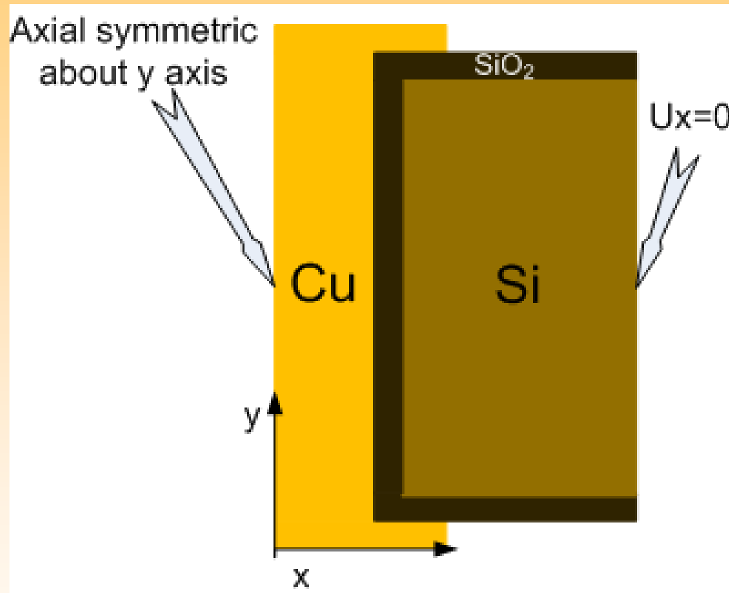
- 2D Fracture Analysis
- 3D Analysis
  - Cu Pumping and Sinking
  - Different TSV Geometries
  - Fabrication-Induced Defects
  - Silicon interposer vs. glass interposer

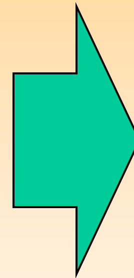
# Material Models

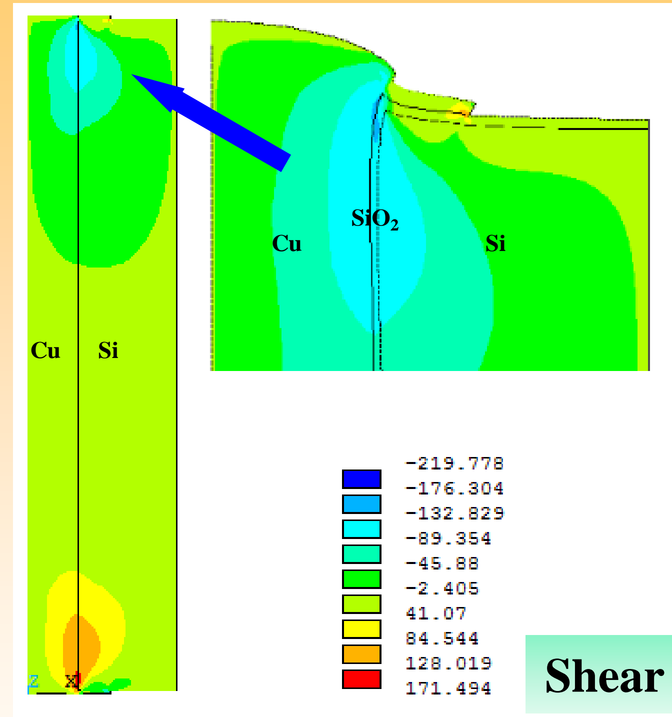
| | Cu | $SiO_2$ | Si |
|---|---|---|---|
| Young's Modulus (GPa) | Table below | 71.4 | 130.91 |
| Poisson ratio | 0.3 | 0.16 | 0.28 |
| CTE (ppm/°C) | 17.3 | 0.5 | 2.6 |

| Temperature (°C) | 27 | 38 | 95 |
|---|---|---|---|
| Young's Modulus (GPa) | 121.00 | 120.48 | 117.88 |
| Temperature (°C) | 149 | 204 | 260 |
| Young's Modulus (GPa) | 115.24 | 112.64 | 110.00 |
| Temperature (°C) | 27 | | |
| Plastic Curve - stress (MPa) vs. strain | 121@ 0.001ε<br>186@ 0.004ε<br>217@ 0.01ε<br>234@ 0.02ε<br>248@ 0.04ε | | |

# Stress and Fracture Analysis



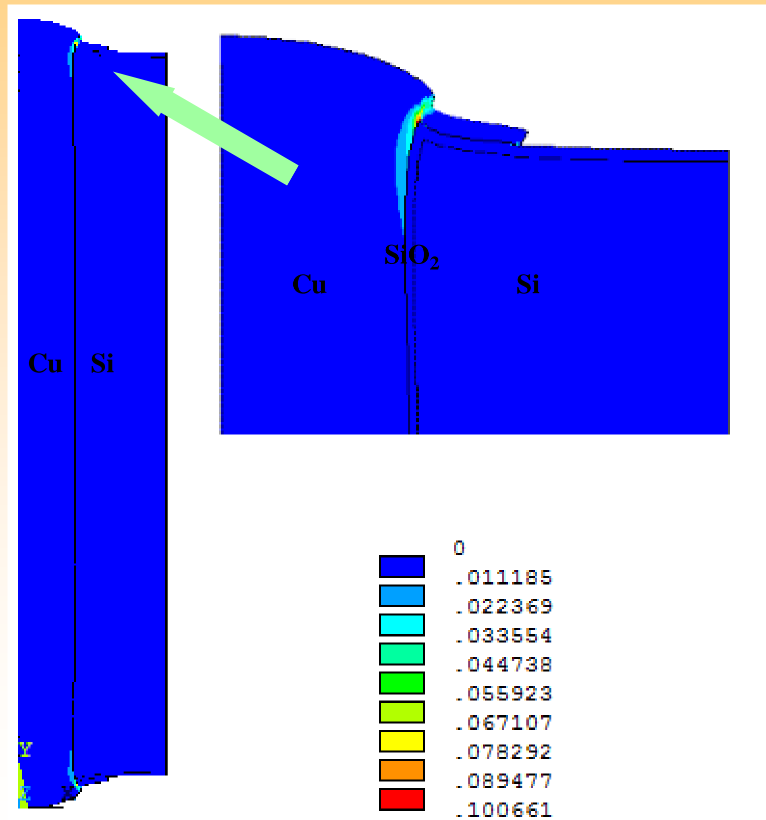






Shear Stress

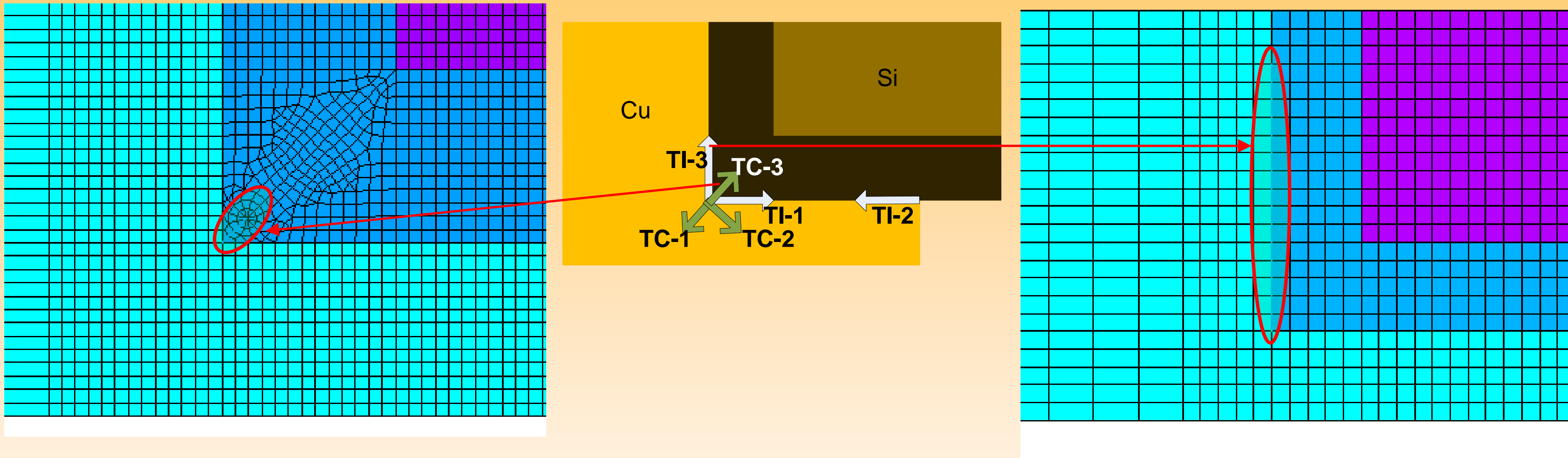
- Axisymmetric model
- Isothermally loaded with the stress free temperature to be 50 C, which was got from XRD measurement
- Large shear stress exist near the corners

# Equivalent plastic strain through via at 300°C




- Cu via yielded near the corners

# Fracture modeling

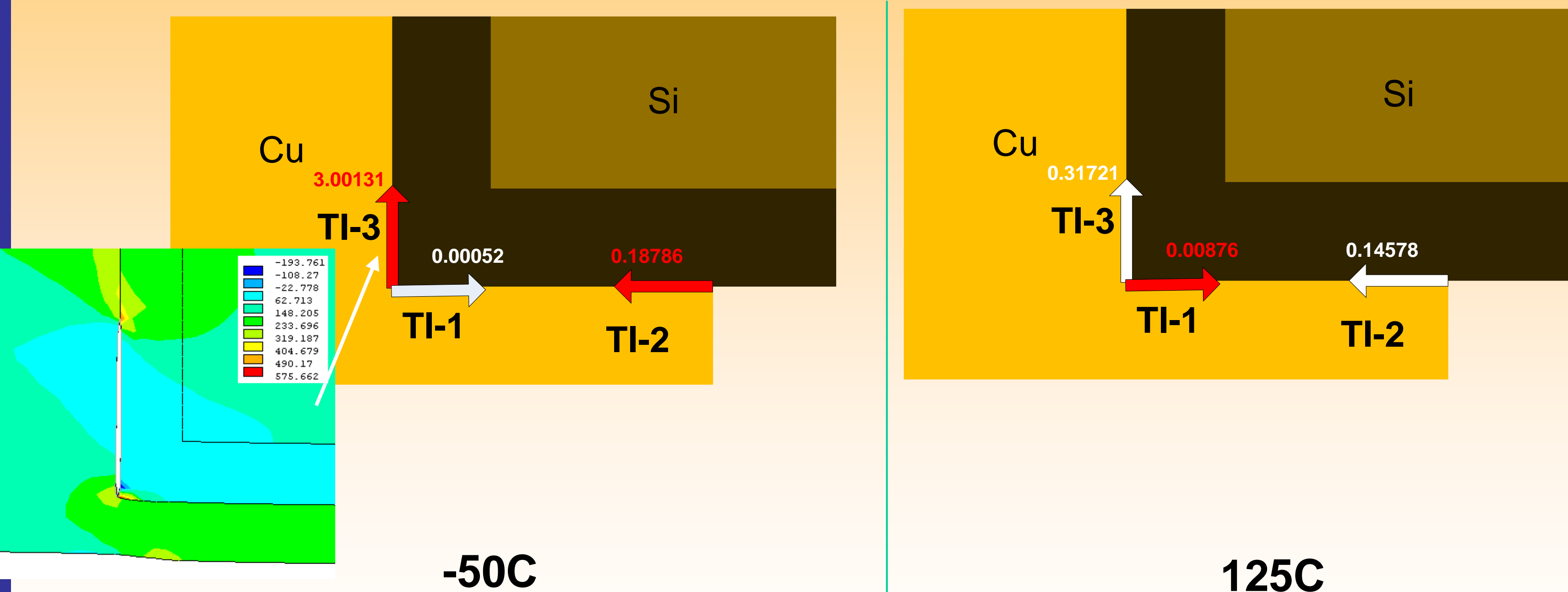



- Assumptions
  - Linear elastic fracture
  - Only one crack (cohesive/interfacial) exists in the TSV at a time; Cohesive crack grows along 45 degrees
- Contact elements to avoid penetration
- Energy release rate G, got by forward finite difference



Note: notation ***T*** represents through-via; ***B*** represents blind-via; ***C*** represents cohesive crack; ***I*** represents interfacial crack.

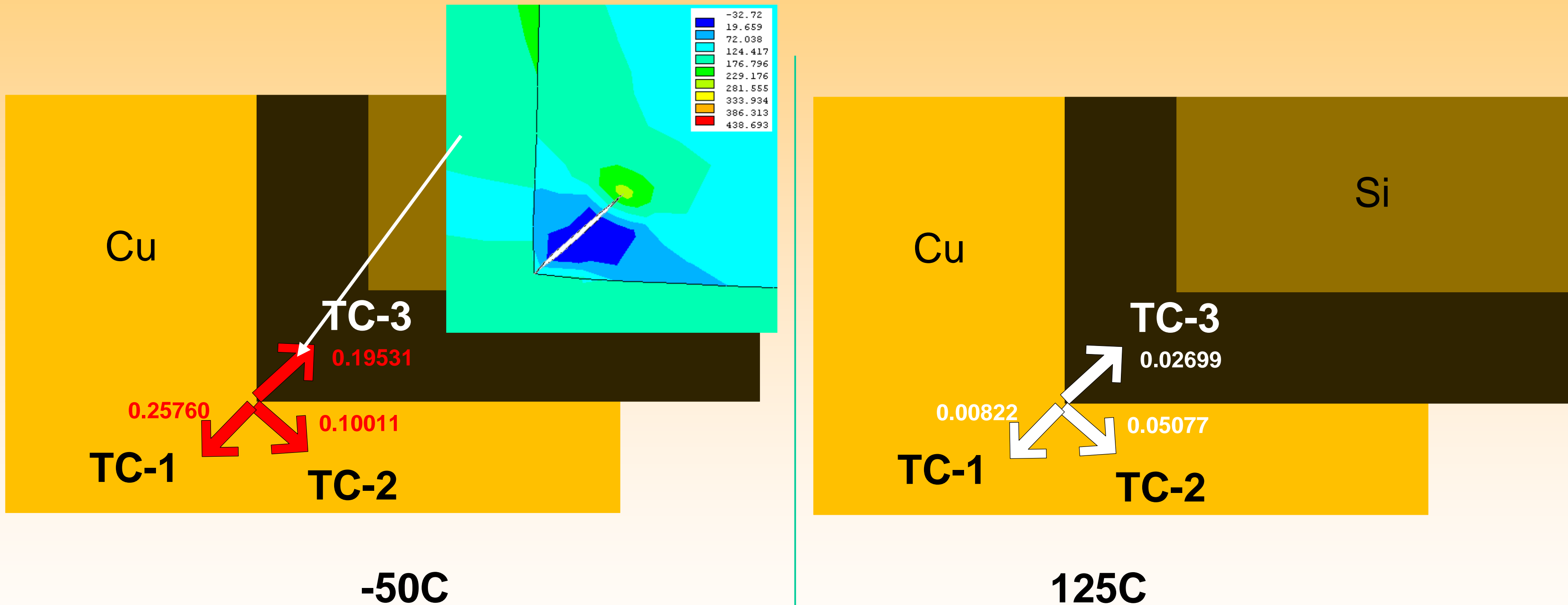
# Energy Release Rate of interfacial crack in Through-via




- Interfacial crack TI-3 is critical in Through-via
- Open crack in one temperature extreme will close on another temperature extreme

Note: red arrows indicate OPEN cracks; white ones indicate CLOSE cracks

# ERR of Cohesive Crack in Through-via




- Cohesive crack TC-3 is the critical in Through-via.
- Although the G value of TC-1 is the largest, cohesive crack is unlikely initiate from here, because the high $G_c$ value of Cu.


- This work is funded by the Semiconductor Research Corporation ; presented at ECTC

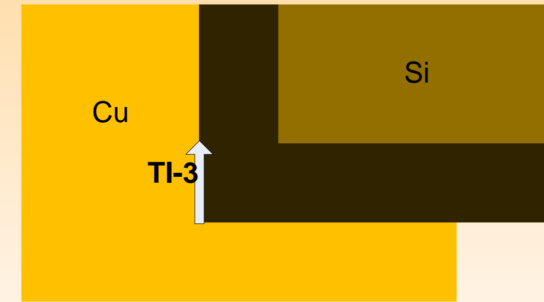
# Crack length vs. G value at TI-3

G (J/m2)

0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00

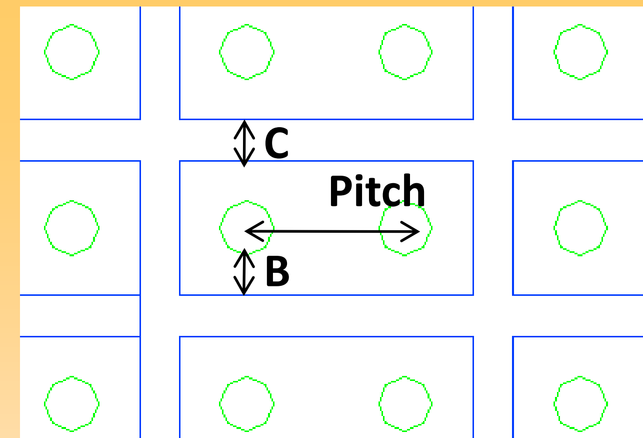
2.5 3 3.5 4 8 10 15

Crack length (µm)




- At TI-3 in Through-via, as crack grows, G keep increasing, results in unstable crack propagation
- Other critical location shows unstable crack propagation

# TSV designs and dimensions




| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C2) | 40 | 30 | 30 | 130 |
| Circle (C3) | 40 | 30 | 55 | 155 |
| Circle (C4) | 65 | 30 | 30 | 155 |

Pitch Effect

Diameter Effect

| TSV | Side (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Square (S) | 57 | 30 | 38 | 155 |

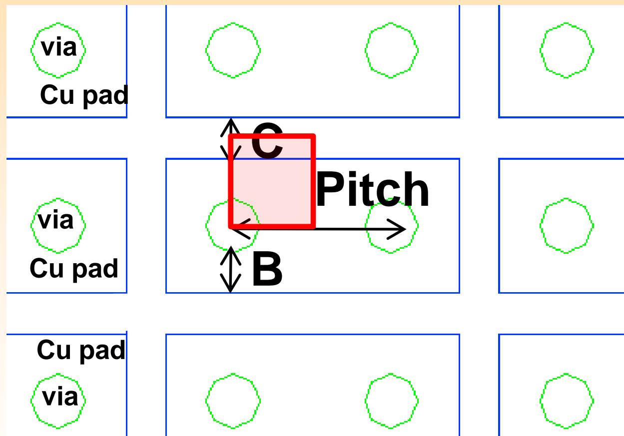
| TSV | Inner Diameter (um) | Outer Diameter (um) | Gap (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|---|---|
| Annular (A) | 25 | 65 | 20 | 30 | 30 | 155 |

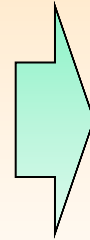
Shape Effect

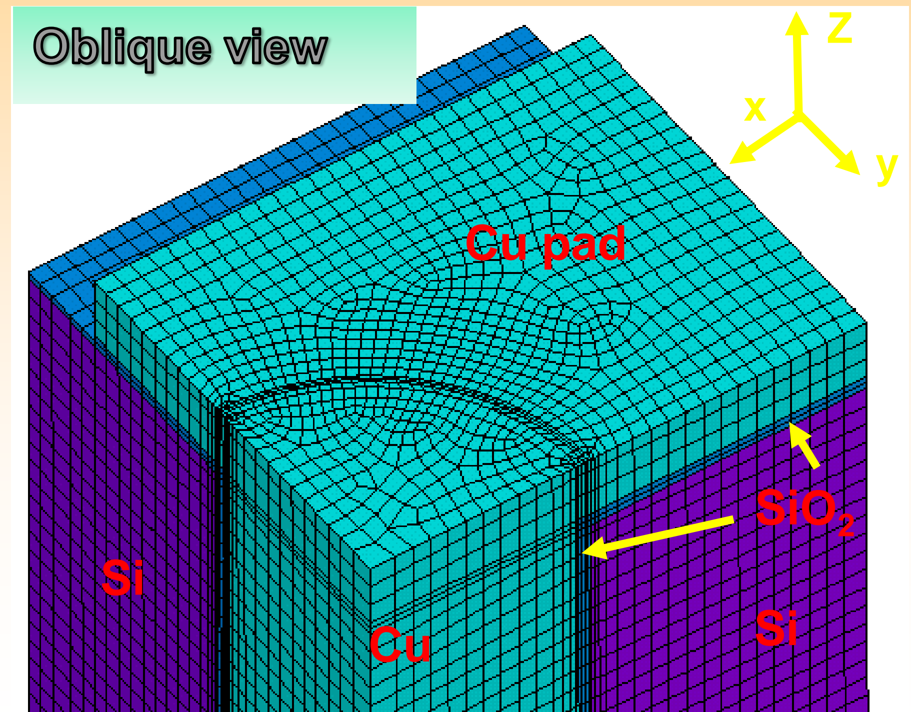
- Above tables show the dimensions of different TSV designs, which will be analyzed and compared in the following FEM analysis

# Circular vias

| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C2) | 40 | 30 | 30 | 130 |
| Circle (C3) | 40 | 30 | 55 | 155 |
| Circle (C4) | 65 | 30 | 30 | 155 |



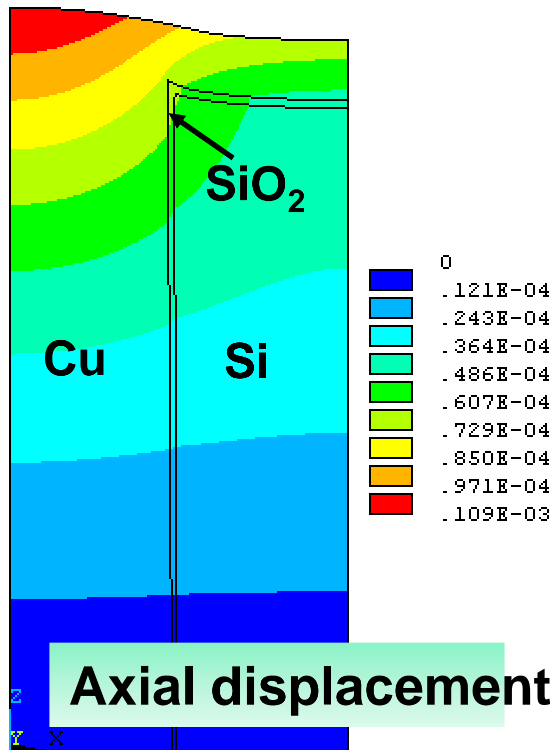



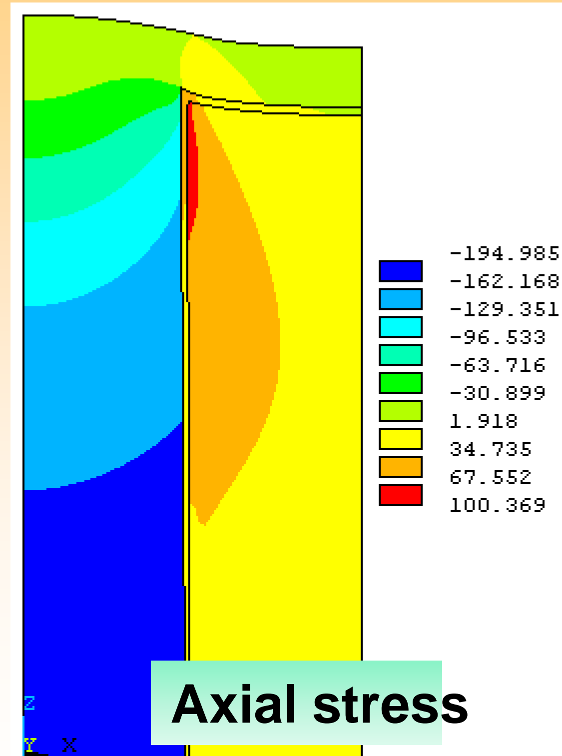



- 1/8 models were built
- Ramp temperature from stress free (50 C) to 125 C
- Design C4 was used to compare with other designs and study the effect of voids and undercutting

# Cu "pumping" at 125 C

| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C4) | 65 | 30 | 30 | 155 |

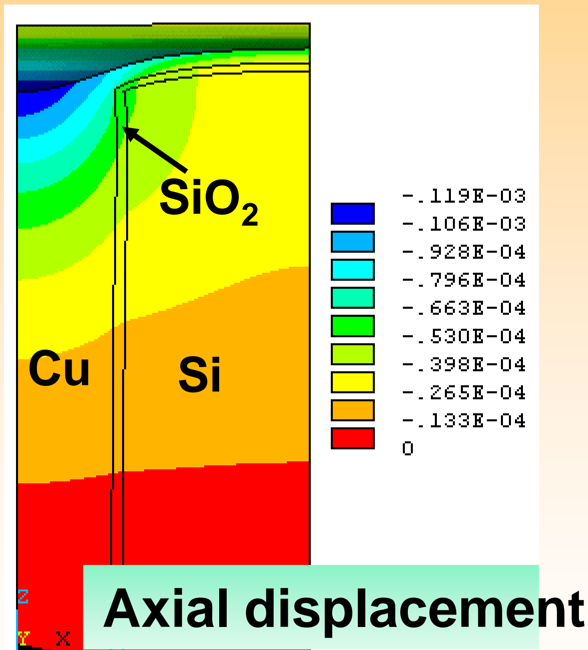


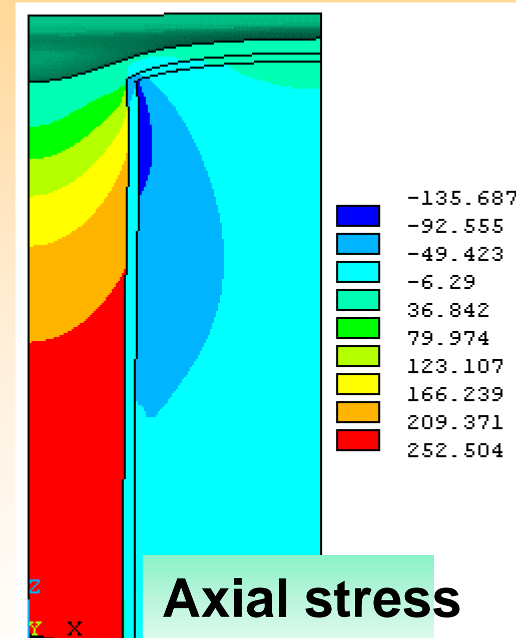




- Cu "pumping" occurs at high temperature (125 C)
- At 125 C, expansion of Cu via is constrained by Si wafer, causing large compression stress at Cu via center and tensile stress in the Si/$SiO_2$
- The differential expansion of Si and Cu via may cause large stress near Cu/$SiO_2$ interface

# Cu "sinking" at -40 C

| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C4) | 65 | 30 | 30 | 155 |



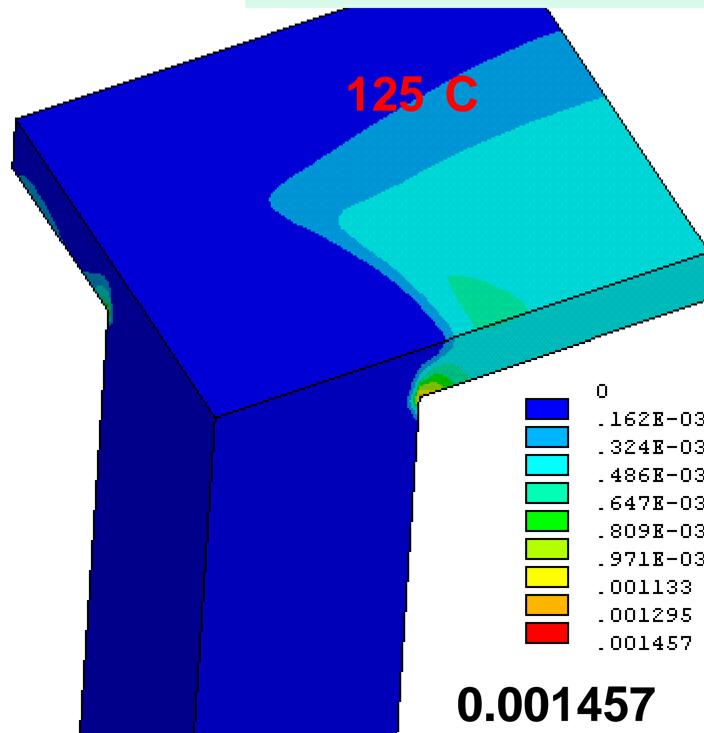



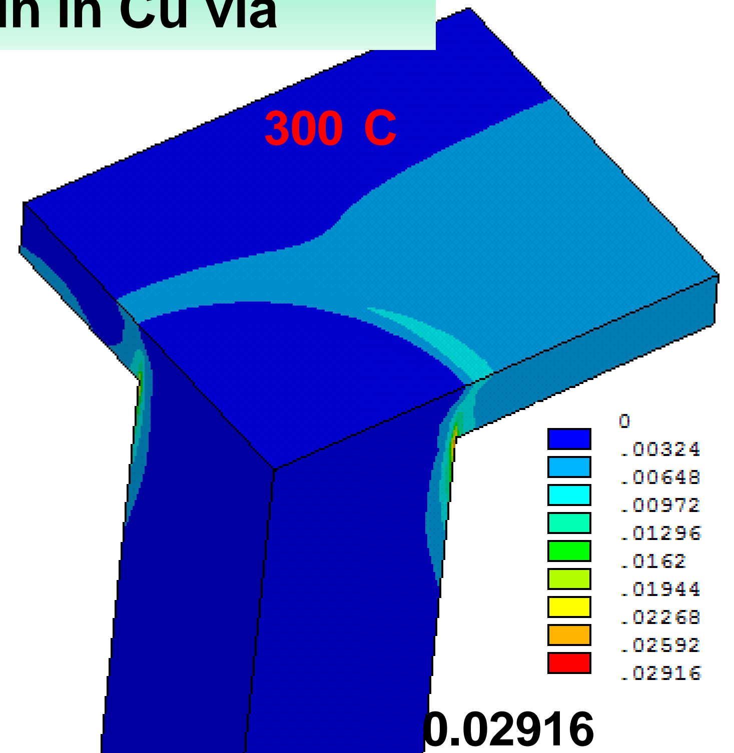

- Cu "sinking" occurs at low temperature (-40 C)
- At -40 C, shrinkage of Cu via is constrained by Si wafer, causing large tensile stress at Cu via center and compression stress in the Si/$SiO_2$
- The differential expansion of Si and Cu via may cause large stress near Cu/$SiO_2$ interface

# Effect of temperature range (cont.)

| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C4) | 65 | 30 | 30 | 155 |

**Equivalent plastic strain in Cu via**

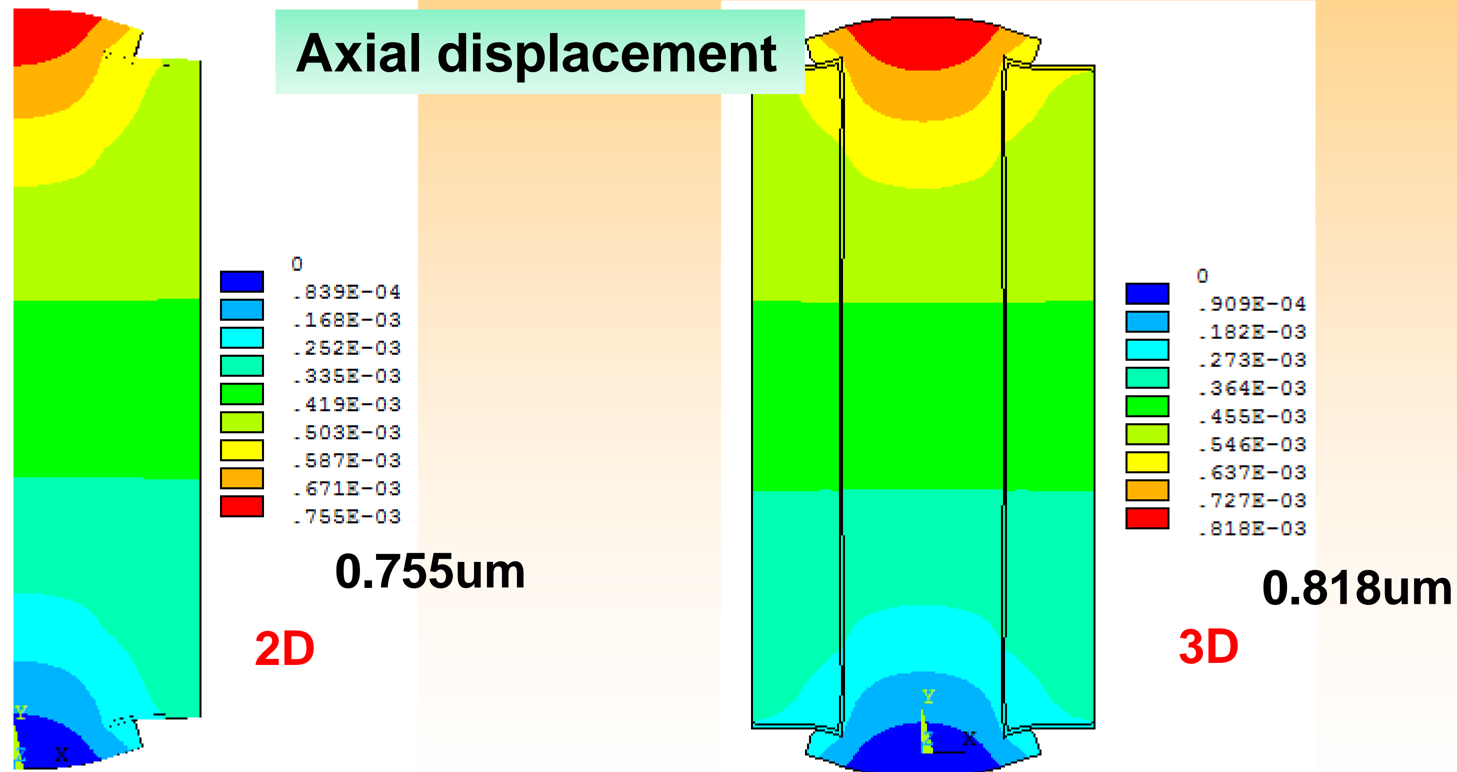



- The plastic strain distribution in Cu is close, indicating the same critical locations (Via upper corner)
- Higher temperature results in much larger plastic strain in Cu

# 2D vs. 3D model (125 C)

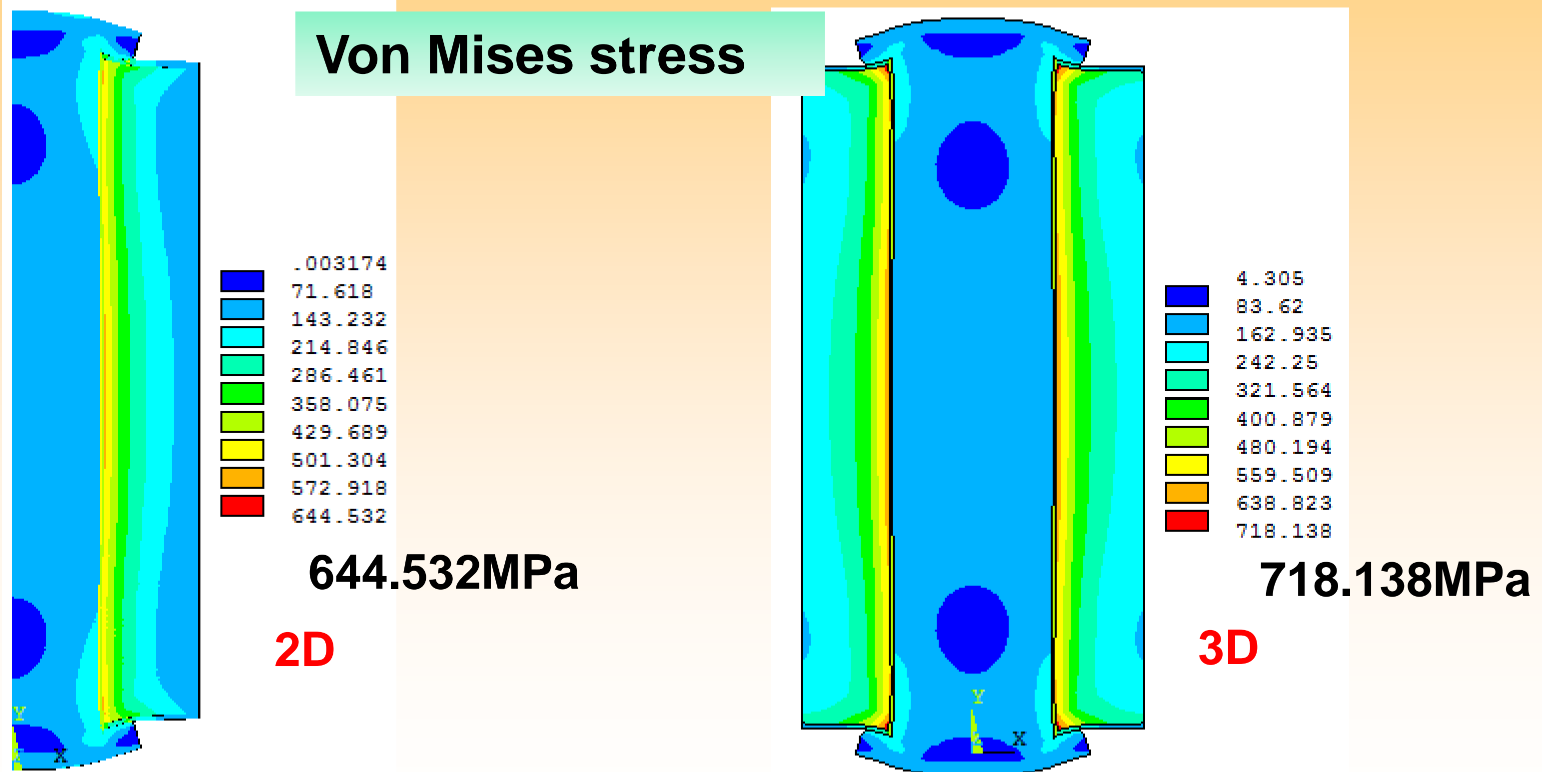
| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C4) | 65 | 30 | 30 | 155 |




- Using 2D (axial symmetric) and 3D models to analyze circular via (C4)
- Both 2D and 3D give similar axial displacement distribution. The magnitude difference is also small, within 10%

# 2D vs. 3D model (125 C)

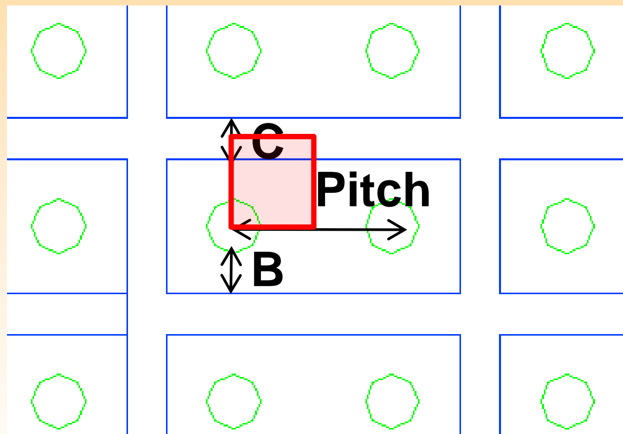
| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C4) | 65 | 30 | 30 | 155 |

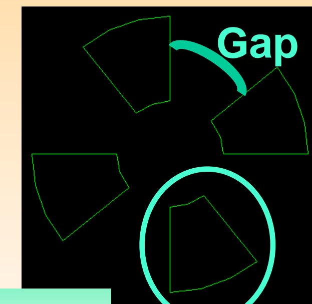


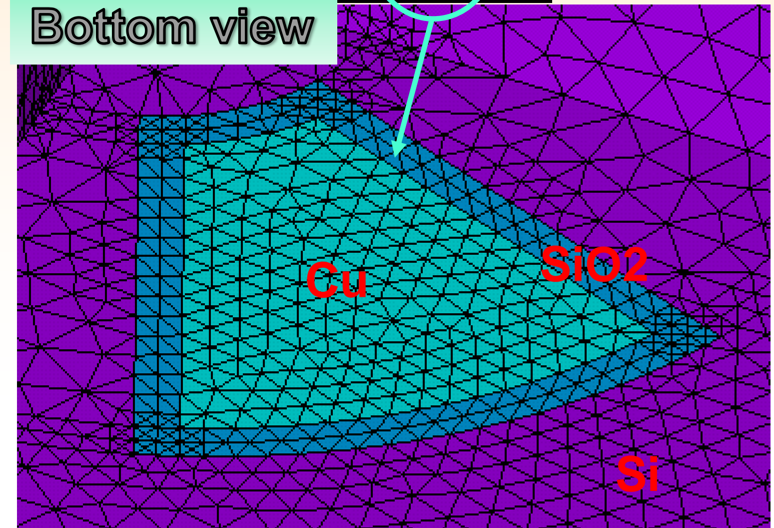

- Both 2D and 3D give similar von Mises distribution. The magnitude difference is also small, within 11%
- <u>2D model can only analyze axial symmetric via (circular-via) with circular pads.</u>

# Annular via

| TSV | Inner Diameter (um) | Outer Diameter (um) | Gap (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|---|---|
| Annular (A) | 25 | 65 | 20 | 30 | 30 | 155 |



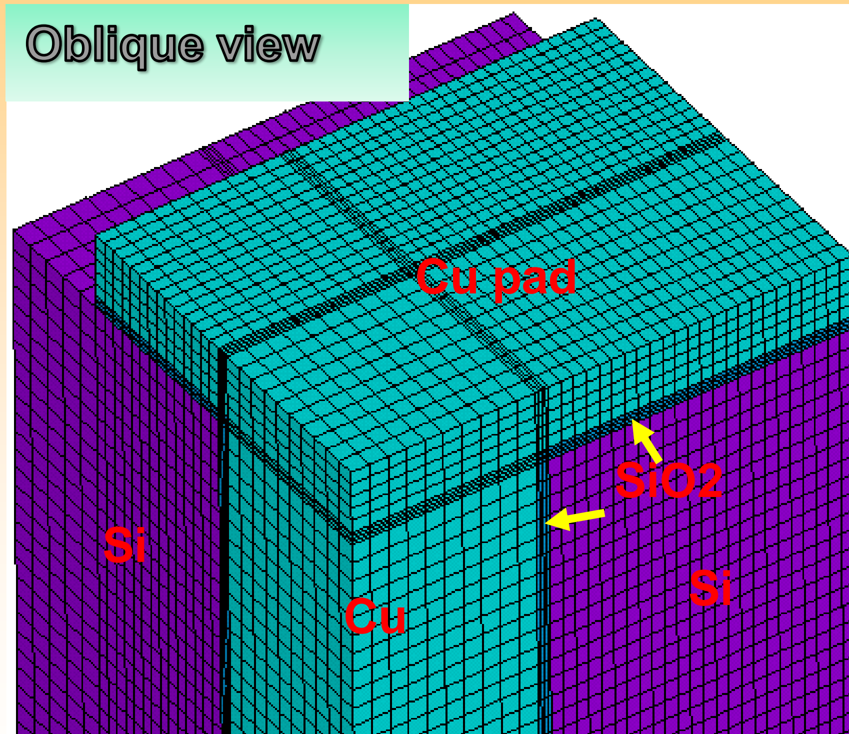




- $1/8^{th}$ models were built
- Ramp temperature from stress free (50 °C) to 125 °C

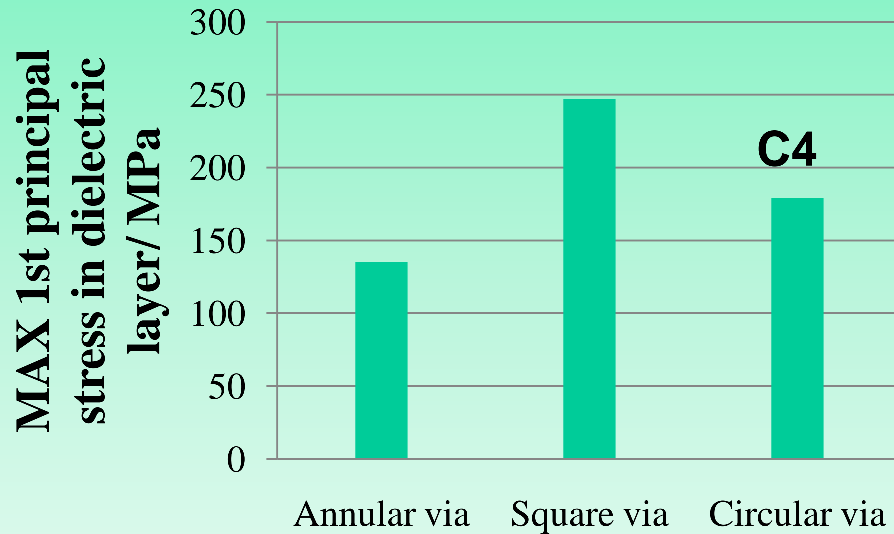
# Square Via Model

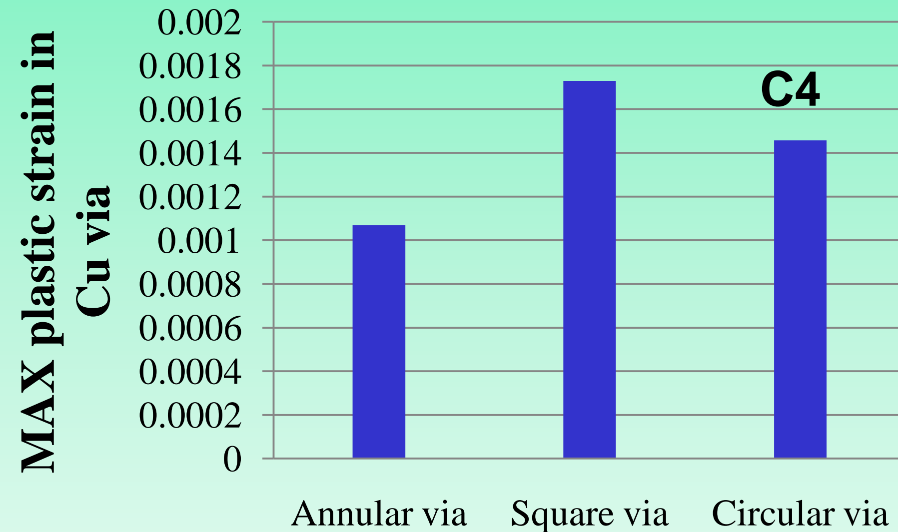
| TSV | Side (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Square (S) | 57 | 30 | 38 | 155 |




- 1/8th models were built
- Ramp temperature from stress free (50 °C) to 125 °C

# Different Via Shapes – Dielectric Stress at 125°C



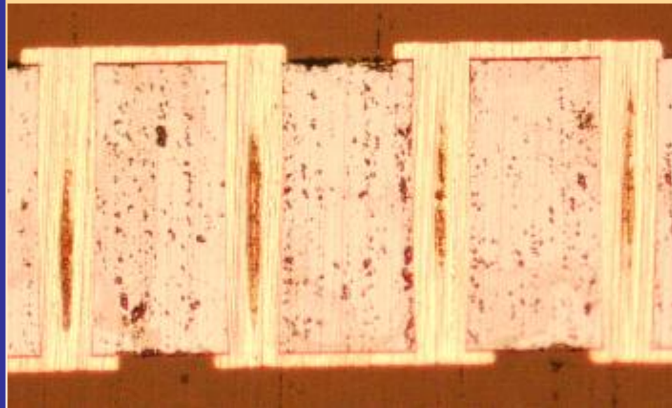



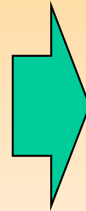

- For vias with the same pitch but deferent shape, the annular via has smallest stress in dielectric layer.
- Square via has the highest stress and plastic strain and more likely to crack dielectric layer and Cu core

# Electroplating and Voids

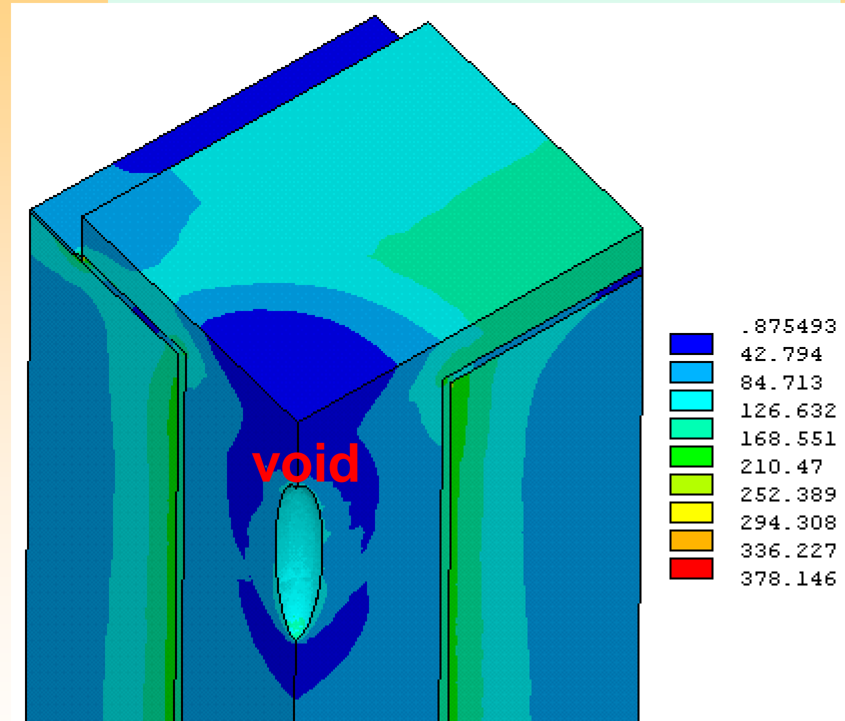
- Although Cu electroplating is well established process used for TSV filling, void-free filling is still a challenge, especially for fast filling and high aspect ratio TSV filling.
- To analyze how those voids will affect the TSV reliability, single elliptical void or randomly generated spherical voids were created within the Cu core.

# Circular via with single void



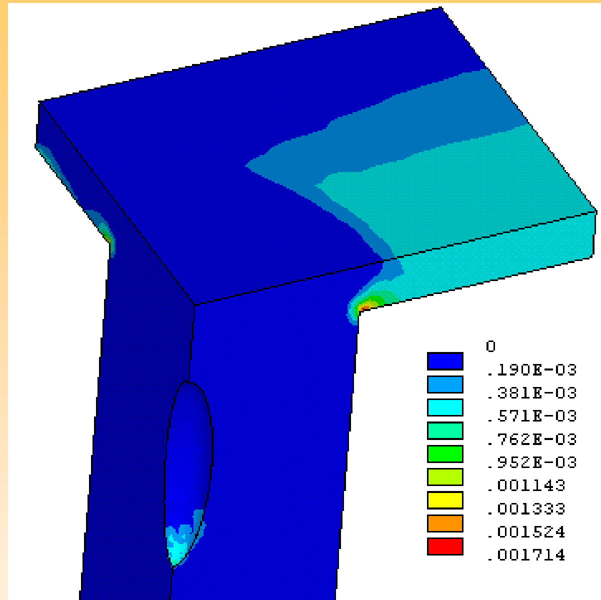


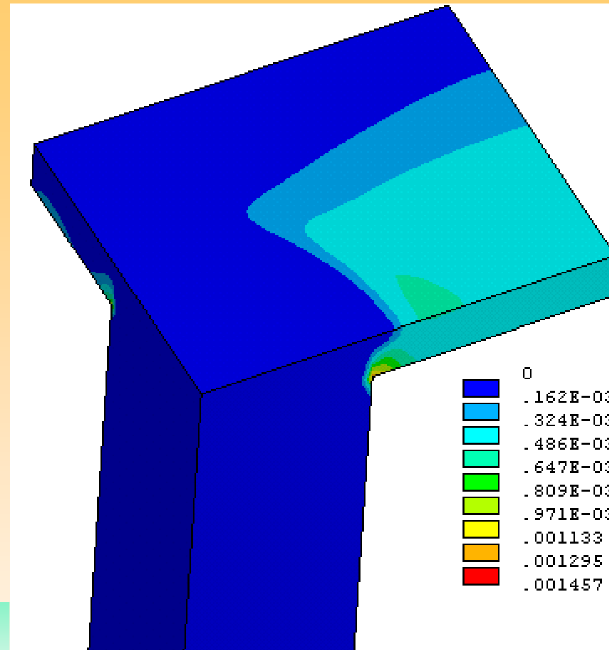
Von Mises stress at 125 C




- 1/8th models were built
- An elliptical void (40um×12um) was modeled in the Cu via to simulate what was observed in actual TSV sample
- Ramp temperature from stress free (50 °C) to 125 °C

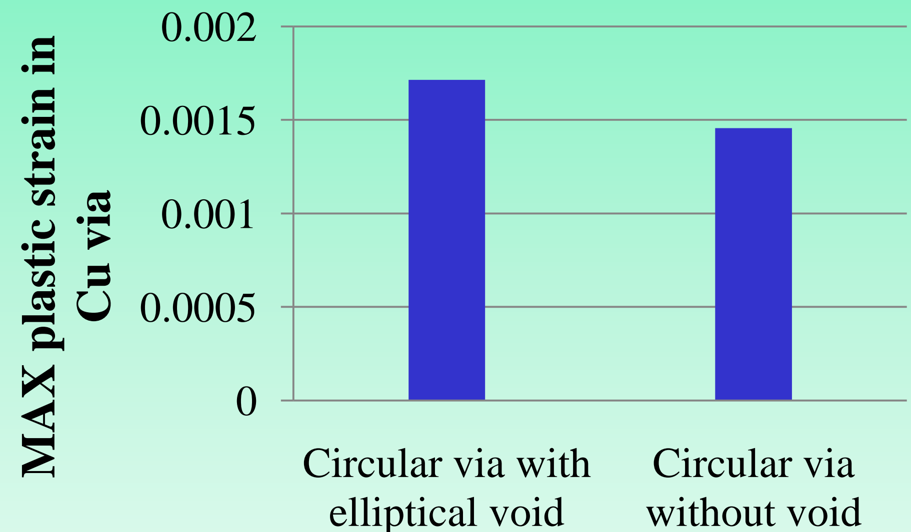
# Plastic strain in Cu via (circular via C4)



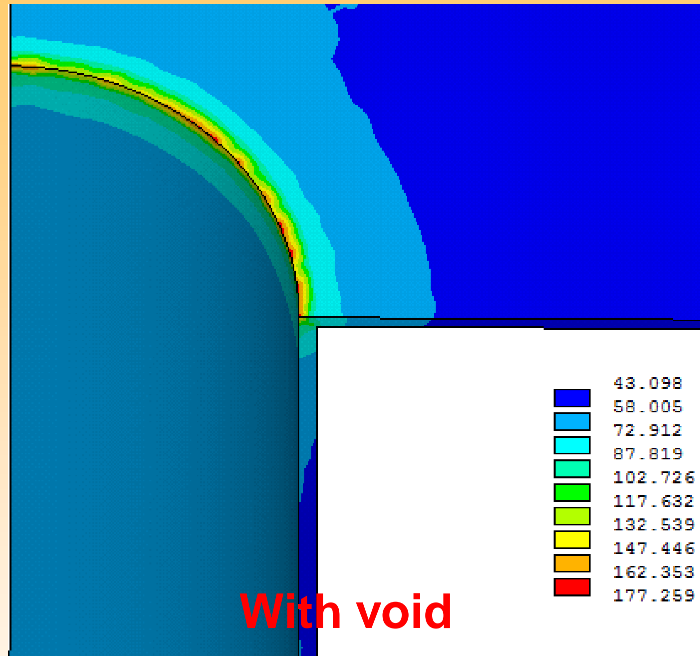



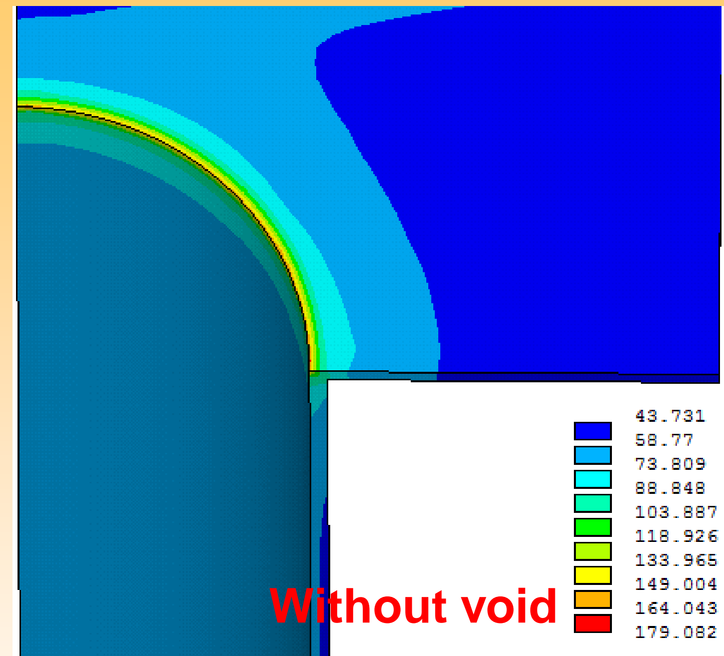

**Equivalent plastic strain at 125 C**

- The elliptical void increases the maximum equivalent plastic strain in the Cu
- Large plastic strain also occurs near the void surface, creating potential fracture initiation spot

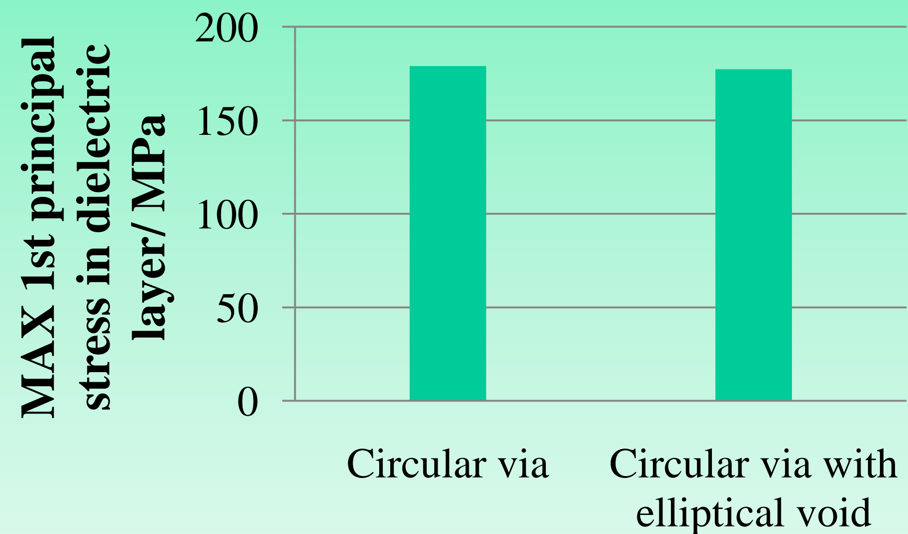


# 1st principal stresses in dielectric layers (circular via C4)

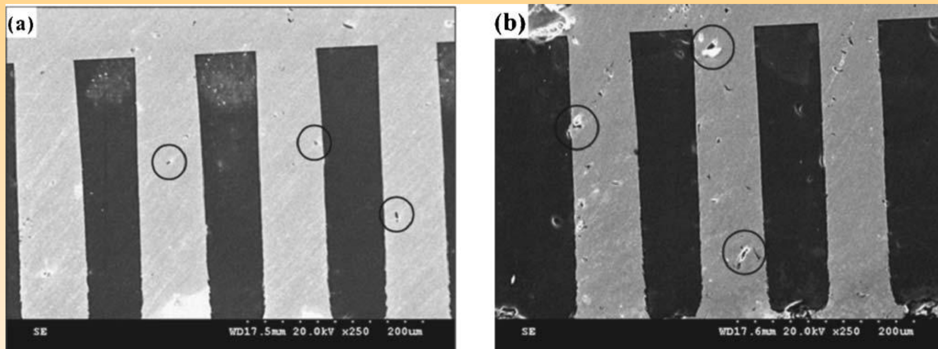


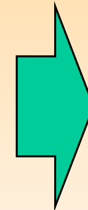

- The void does not obviously change the 1st principal stress distribution in the dielectric layer.
- The existence of void alleviates the stress in the dielectric layer, but the change is limited.

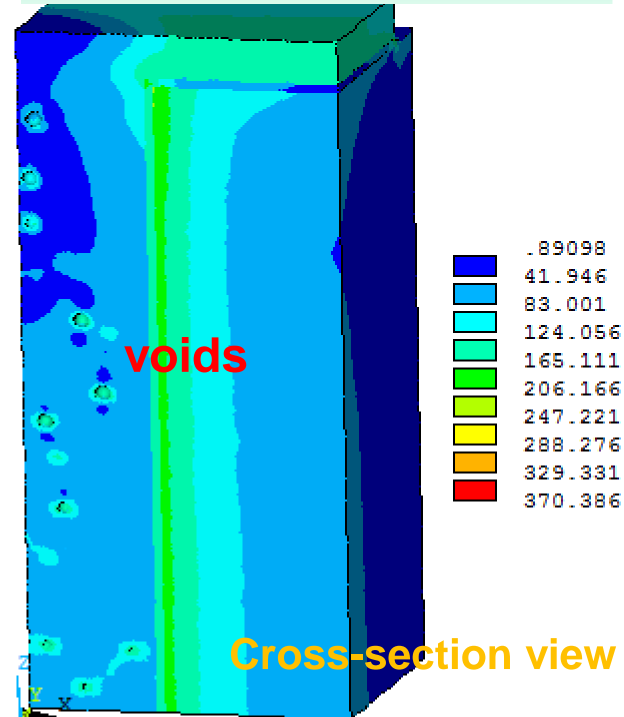


# Circular via with voids



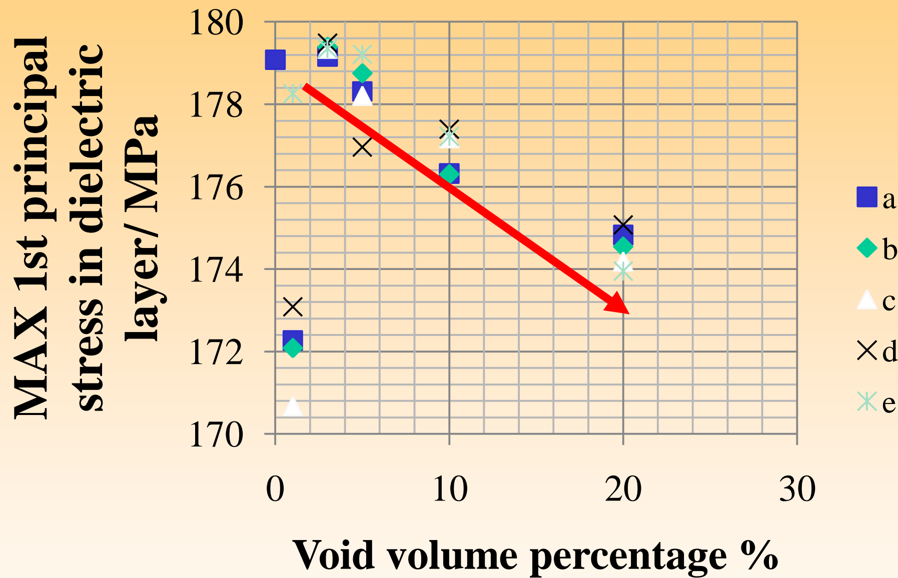

Pradeep Dixit and Jianmin Miao, Aspect-Ratio-Dependent Copper Electrodeposition Technique for Very High Aspect-Ratio Through-Hole Plating

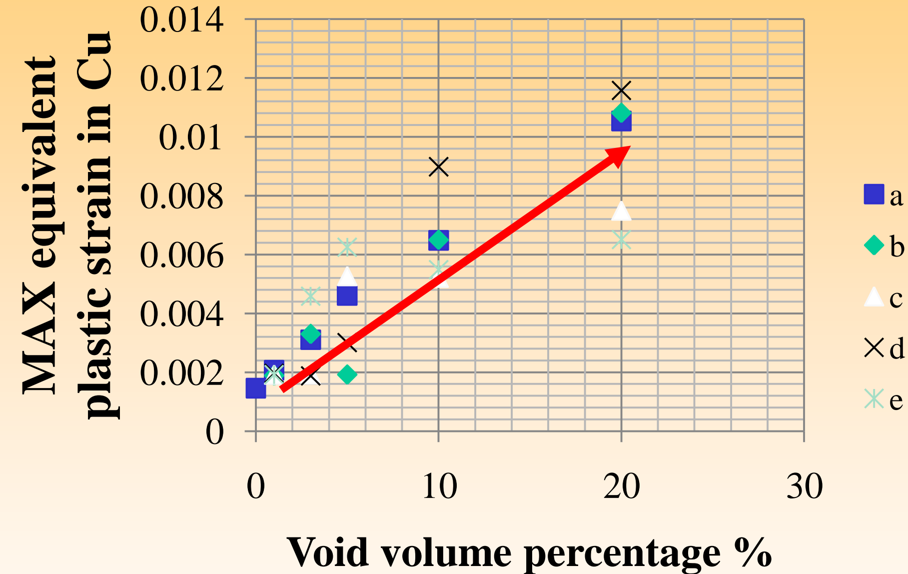





- 1/8th models were built
- Random distributed sphere voids in Cu were modeled
- Ramp temperature from stress free (50 C) to 125 C

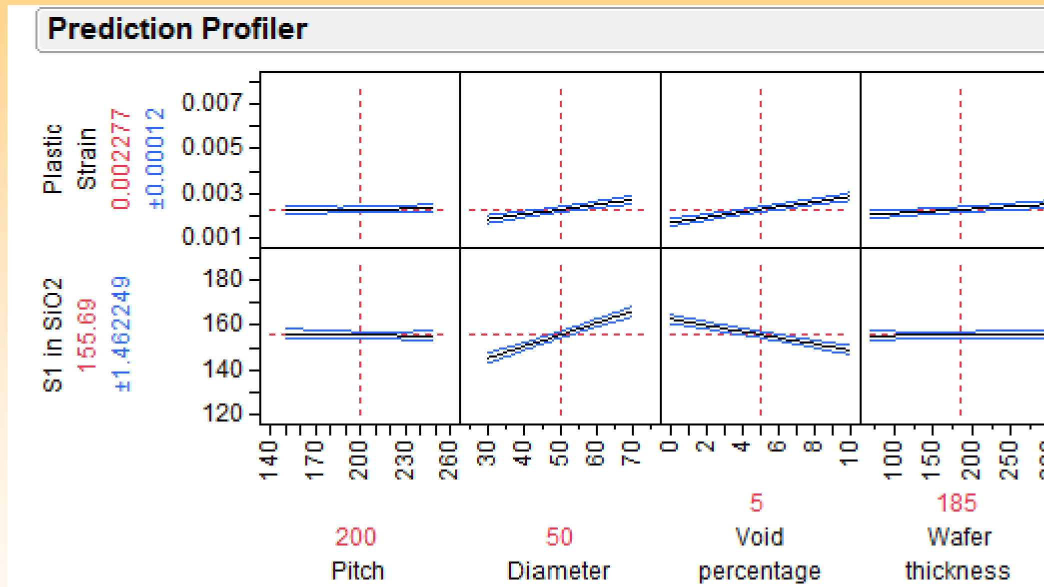
# Effect of void percentage (Circular via at 125 C)



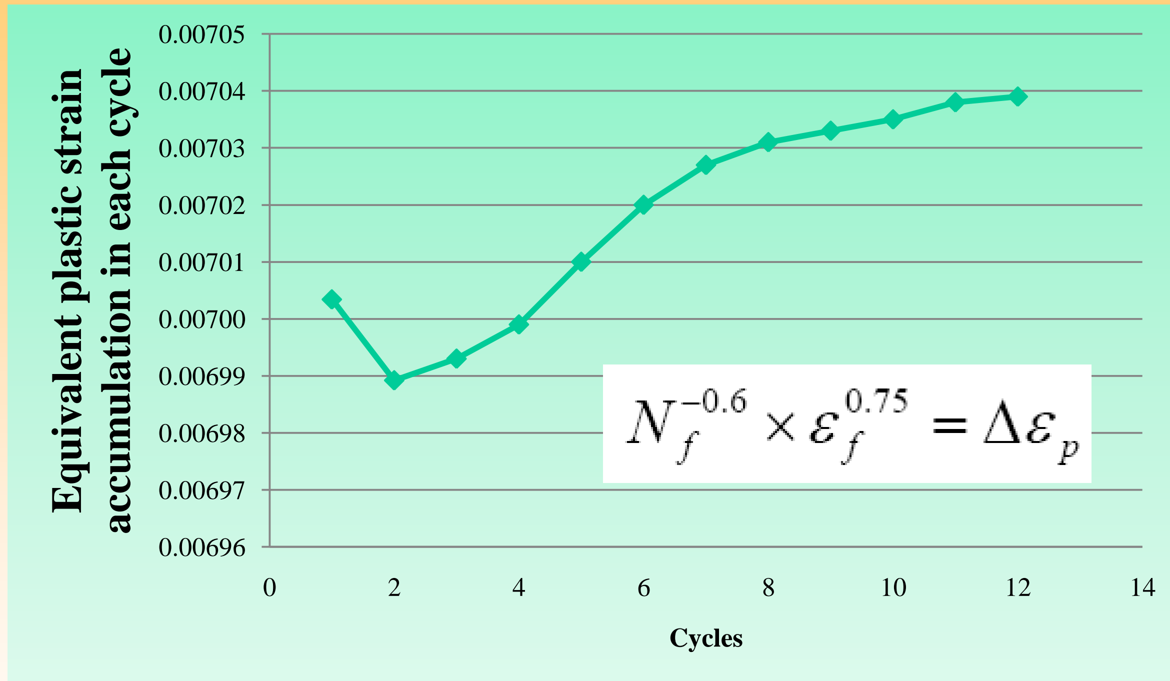

- Fix void radius as 3um, change void volume percentage. For each percentage, five cases were analyzed.
- 1st principal stress in dielectric layer top corner generally decreases when voids occur (compare to no void case), with large scatter as void percentage is low (1%).
- MAX plastic strain in Cu vias increases as void percentage increases

# Design parameter effects




- Both plastic strain in Cu & principal stress in $SiO_2$ increase with larger diameter
- The existence of voids decreases the stress $SiO_2$, however, increases the plastic strain in Cu
- The effect of wafer thickness and pitch on the stress/strain is small

# Cu via fatigue life prediction




- Plastic strain accumulated in each cycle stabilized after 12 cycles, being about 0.00703, therefore, strain range is 0.003515
- Base on previous Coffin-Manson type equation, fatigue life of Cu via is more than 2700 cycles

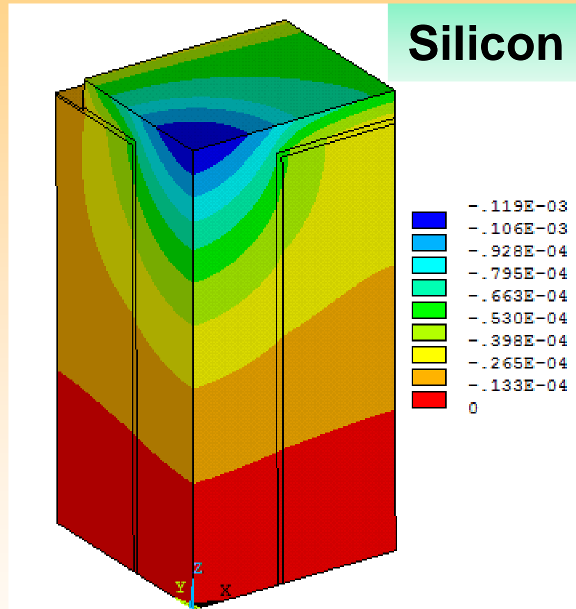
# Silicon interposer vs. Glass interposer

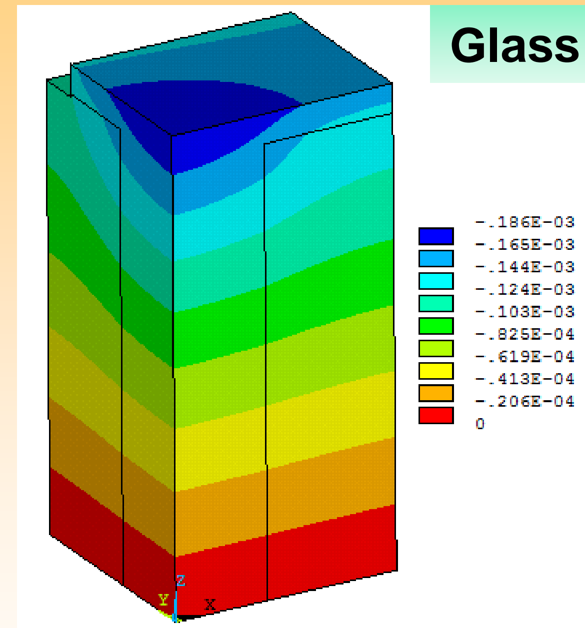
| | E (Gpa) | Poisson ratio | CTE (ppm/ºC) |
|---|---|---|---|
| Glass | 71 | 0.24 | 8.5 |

| TSV | Diameter (um) | B (um) | C (um) | Pitch (um) |
|---|---|---|---|---|
| Circle (C4) | 65 | 30 | 30 | 155 |

- To make glass and Silicon interposer models comparable, the same geometry is used (C4)
- Thermo-mechanical properties of Silicon and other materials are given earlier

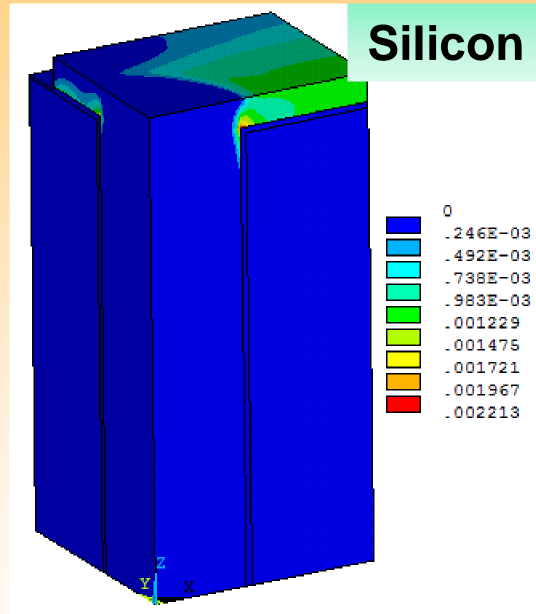
# Silicon interposer vs. Glass interposer Out of plane displacement $U_z$ @-40ºC

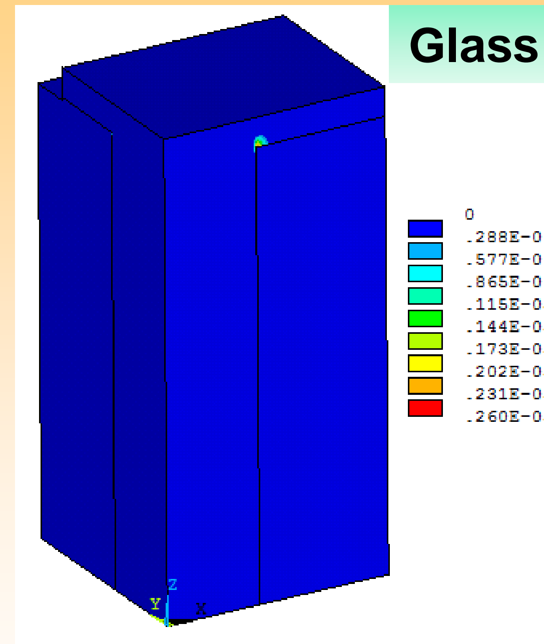



- Glass interposer has higher CTE than Silicon. The overall out of plane displacement of glass interposer is larger
- Glass interposer has less CTE mismatch with Cu than that of Silicon interposer, resulting in more uniform displacing contour

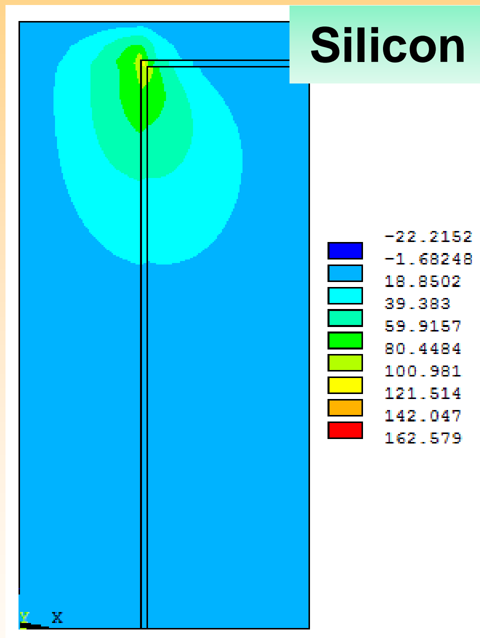
# Silicon interposer vs. Glass interposer Equivalent plastic strain@-40ºC

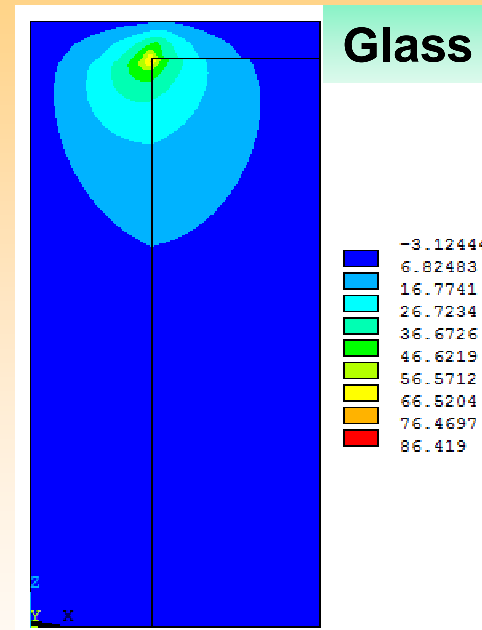



- Glass interposer has less CTE mismatch with Cu than that of Silicon interposer, resulting in less plastic deformation in Cu via

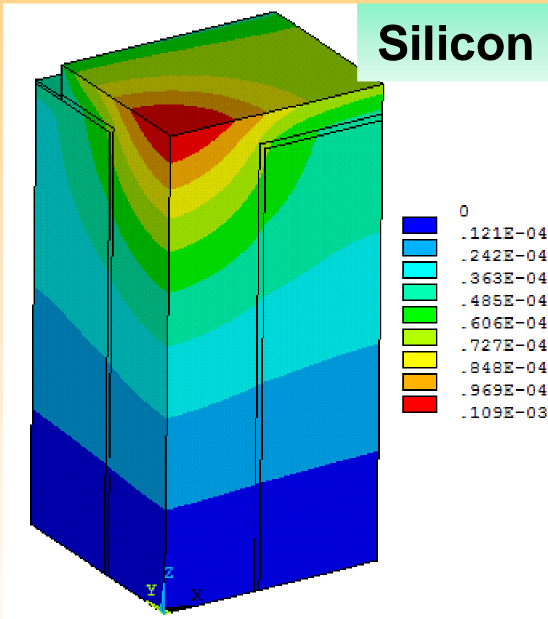
# Silicon interposer vs. Glass interposer shear strain @-40ºC

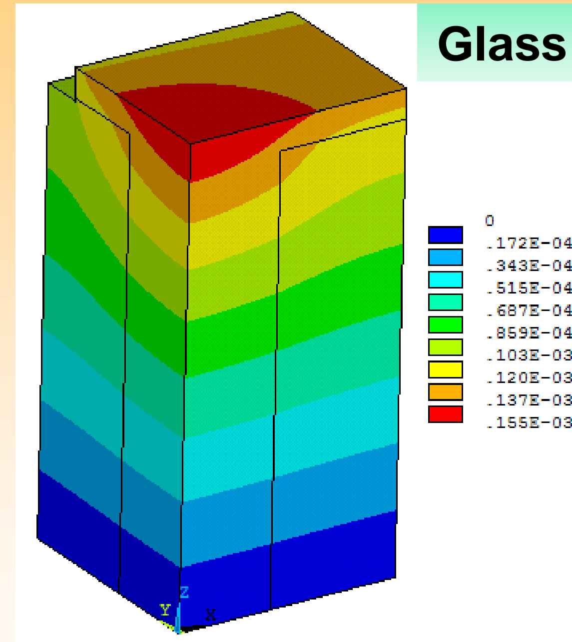



- Glass interposer has less CTE mismatch with Cu than that of Silicon interposer, resulting in less shear strain near the corners

# Silicon interposer vs. Glass interposer Out of plane displacement $U_z$ 125$^o$C




- Glass interposer has higher CTE than Silicon. The overall out of plane displacement of glass interposer is larger
- Glass interposer has less CTE mismatch with Cu than that of Silicon interposer, resulting in more uniform displacing contour
- Stress/strain in the glass interposer are also smaller at high temperature

# Summary

- Cu pumping/sinking is a concern with Cu burden
- Annular and circular vias are preferable over square vias
- In the selected design parameter range, the effect of wafer thickness and pitch on stress/strain is small
- Voids in Cu help against dielectric cracking; however, Cu cracking will be a concern
- Glass interposer results in better thermo-mechanical performance
- Experimental validation of the failure mechanisms is ongoing