# Thin Passive Components (TPC)

## *Passive Component Integration in* ***Organic, Silicon and Glass Substrates***

*presented by*

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Atlanta, Georgia
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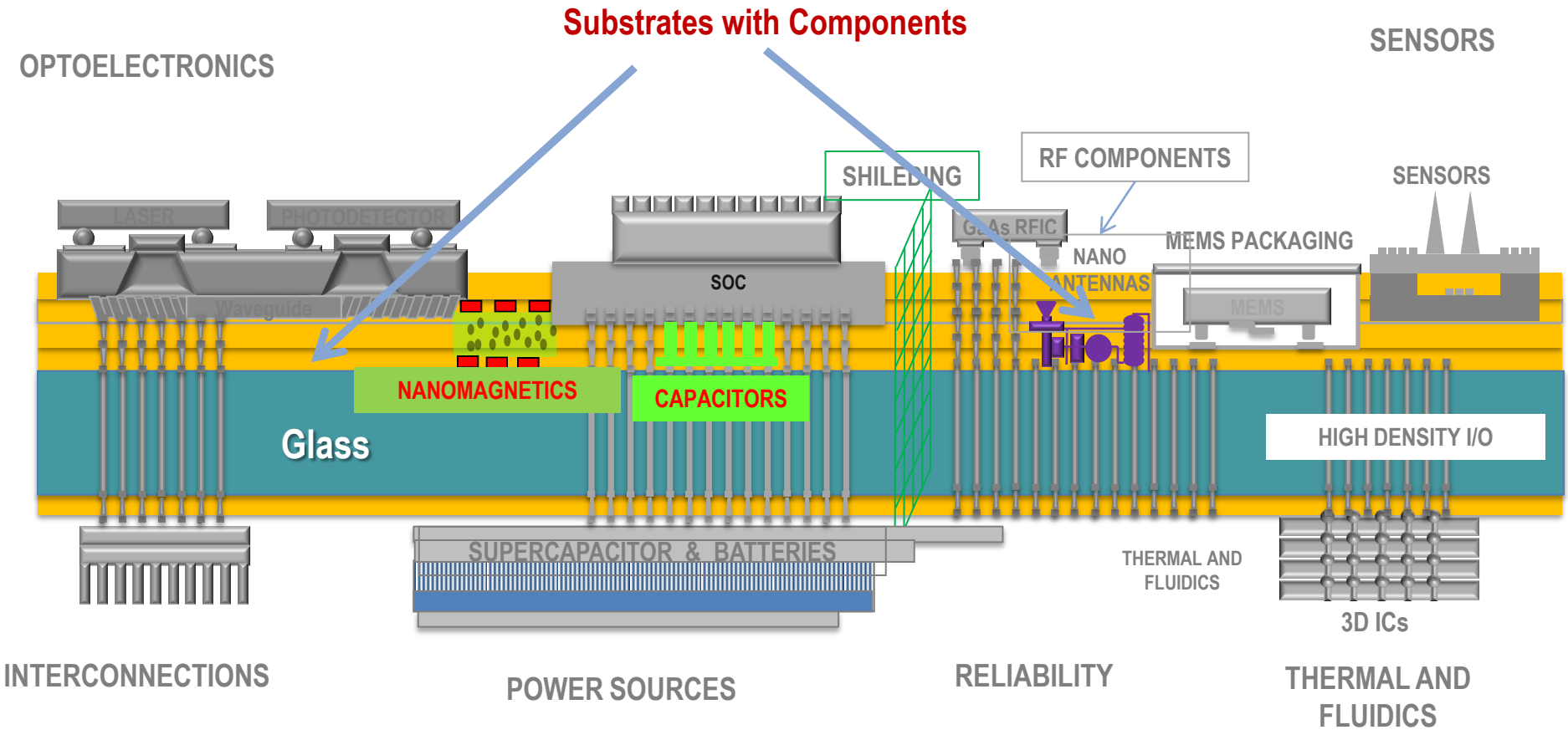
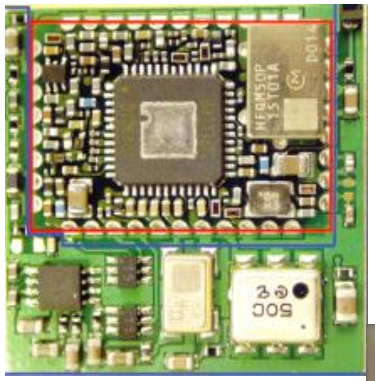
# Research Focus



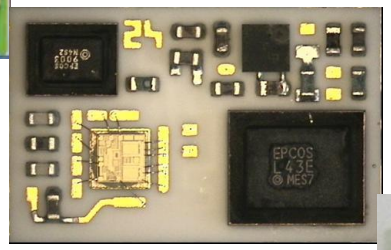
# Passive Component Integration Objectives

- Form factor reduction
  - X, Y and Z (<50µm)
  - Increasing drive to integrate passives at package level rather than board level
- BOM reduction
  - Multi-component IPDs and embedded passives
- Manufacturability and Cost
  - Testability
  - Reparability
  - Focus on high yielding processes

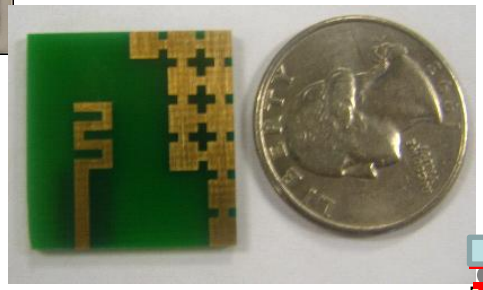
# Passive Component Integration Options



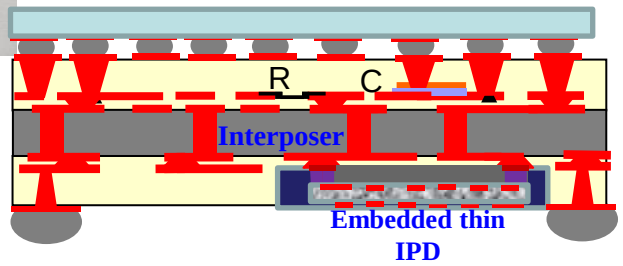
SMT
Discretes



Embedded
Ceramic



Embedded
Organic




TPC Focus – Si, Glass &
Organic IPDs or Embedding

# Passive Integration Challenges

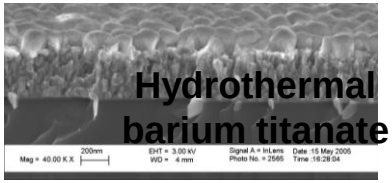
- **Limitations of Current Passive Components:**
  - Thickness incompatibility with thin substrate roadmap
    - 100s of microns to mm vs. organic substrates <200um
  - Area Density limited for ultra-thin form factors
  - Parasitics from interconnects (SMT at board or package level)
  - Pick and place cost for individual passive discrete components

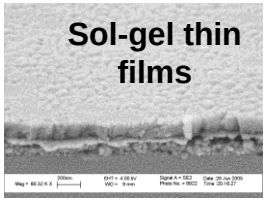
- **Manufacturing Challenges for Integrated Passives:**
  - Low cost test
  - Lack of reparability for integrated passive components
  - Tunability at system level

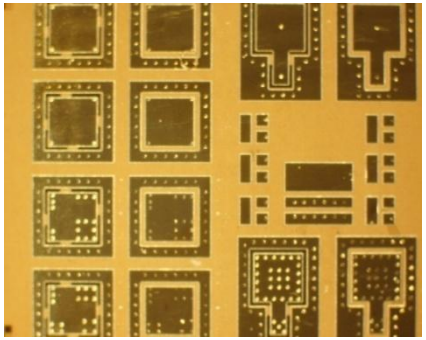
# Component Integration Approaches

- Ultra-Thin Glass or Silicon Interposer for integration of capacitors and magnetic components
- Substrate-compatible high precision RF components
- Embedded thin IPDs in the package substrate with testability and reparability

# Background Research - Integration of Thin Film Decoupling Capacitors in Organic Substrates



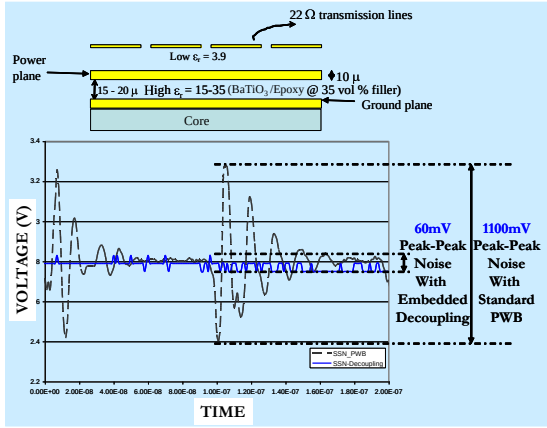



**Large area demonstration of embedded**

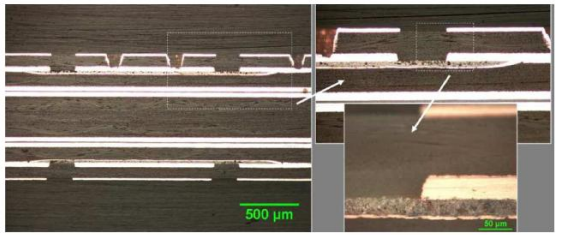
**thin film capacitors on organic board**;

**Nano-Composites & Nano-scale Thin Film High K Materials**




**Industry Prototypes**

**System-Level Function Enhancement**




**DuPont**

*J. Amer. Ceram. Soc., August,* , 93 (9), 2764-2770, 2010 ,

*IEEE CPMT Transactions on Adv. Pkg, Dec. 2007, pp. 585-594.*

Georgia Tech PACKAGING RESEARCH CENTER

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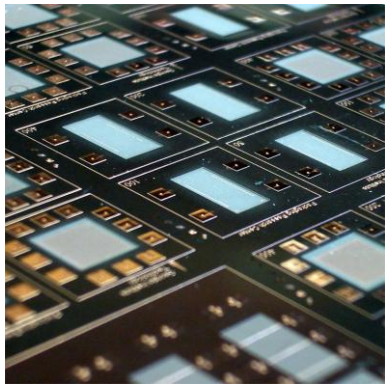
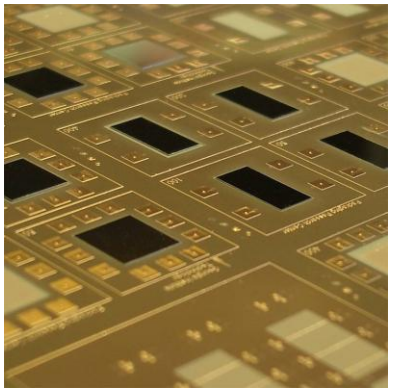
# Component-Last Embedding for Reparability

- Thin IPDs pre-tested
- Low Cost Panel Level Embedding
- Integration processes for:
  - No degradation in yield or electrical performance
  - Thermomechanical compatibility;

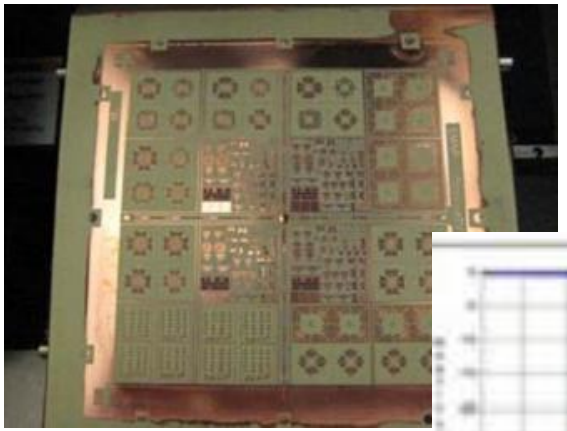


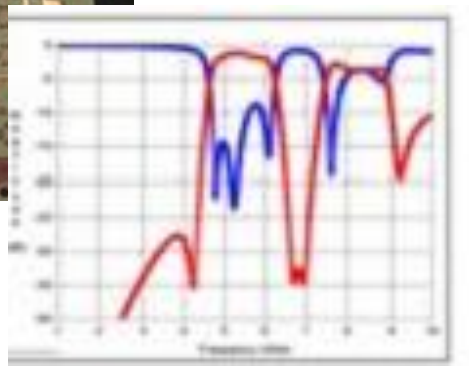


PRC's background in embedded thin discretes

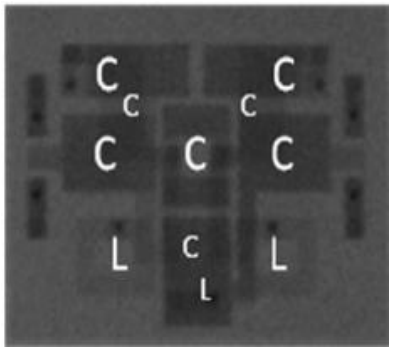
# RF Component Integration

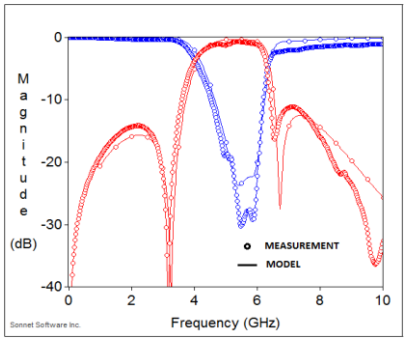
- Organic Substrates
  - Low loss up to 110GHz
  - FR-4 compatible process
  - Ultra-thin (<150µm)





- Inorganic Substrates
  - High precision (<10µm lines/spaces)
  - Ultra-thin and low loss
  - High temperature process compatible

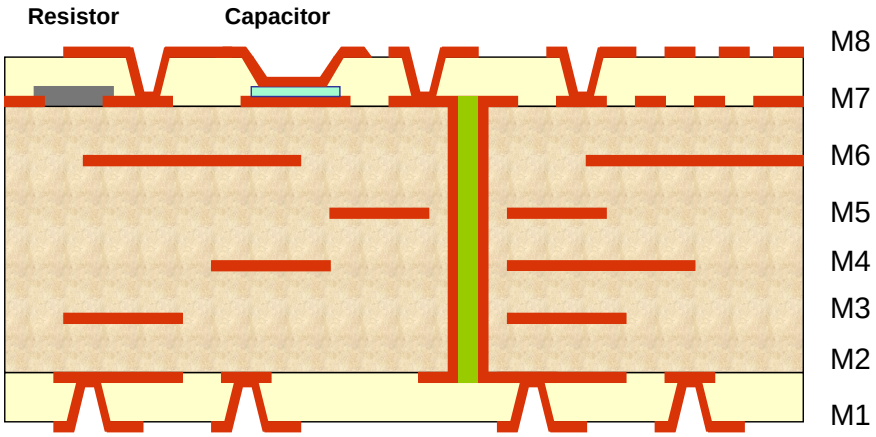


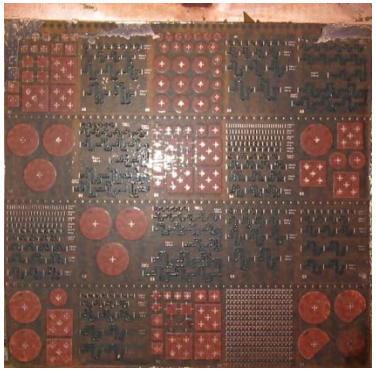



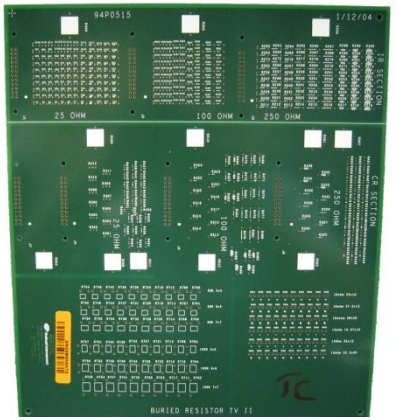

Insertion Loss ~0.72dB

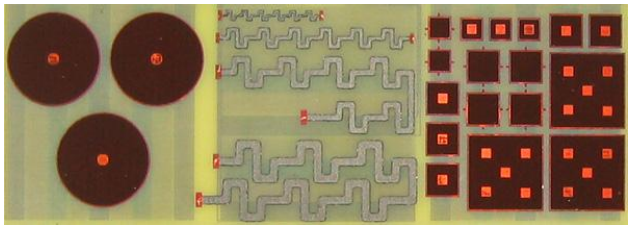
# Industry Prototypes: Nokia Embedded R-C Test Vehicle

- Two year program to explore embedded passives for mobile phone integration







| Test Cases | Temperature range | Soak Time | Humidity | Total Cycles/Hrs |
|---|---|---|---|---|
| Thermal Shock | -55 to 125 $^{o}$C | 10 minutes | N/A | 1000 cycles |
| Temperature Humidity 1 | 85 $^{o}$C | N/A | 85 % | 100 hours |
| Temperature Humidity 2 | 121 $^{o}$C | N/A | 100 % | 1000 hours |


# TPC Workshop

# MAY 25, 2011

*Thank you for attending.*