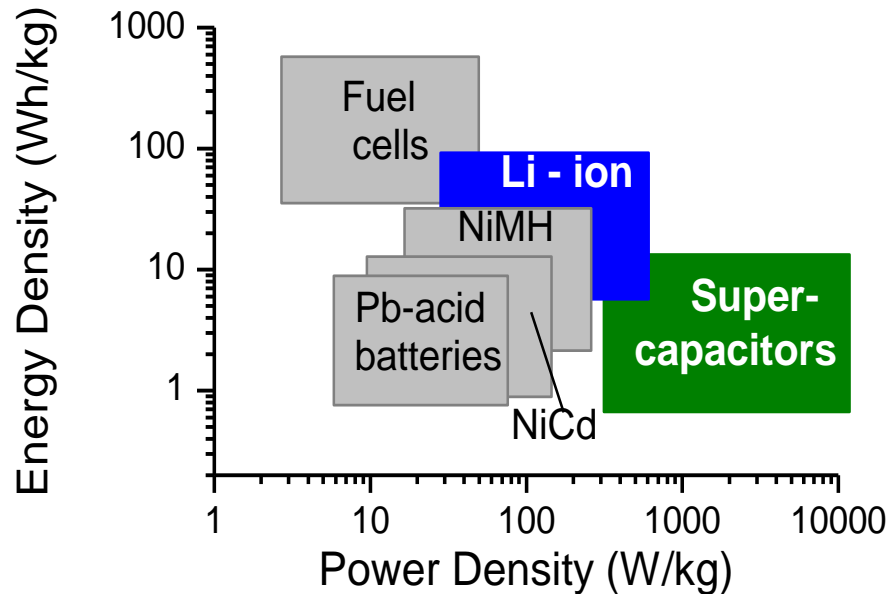


IV. Supercapacitors



conventional



- **Charge storage:**
 - electrical double-layer (EDLC)
 - fast and reversible faradaic redox reaction (pseudocapacitance)
- **Energy storage depends on the ability of electrode to adsorb electrolyte ions under the applied potential**

Advantages over batteries (for conventional device geometry):

- **Higher power**
- **Faster charging** (subseconds/seconds vs. minutes/hours)
- **Less harmful** (no heavy metals)
- **Offer long cycle life** (>1,000,000 cycles vs. 500)
- **Easy to detect the state of charge**
- **Lower fundamental limit for the device voltage** (voltage only restricted by the decomposition of the electrolyte)

What are the fundamental limits of energy storage ?

1. Empirical estimation:

Energy in supercapacitor device $E \approx \frac{CV^2}{2} \cdot \frac{1}{16}$ due to packaging, two C in a series etc.

Capacitance: (a) 6-30 uF/cm² in carbon; (b) up to 200 uF/cm² in functionalized carbon;
(c) up to 200 uF/cm² in transition metal oxides

If surface area = 2000 m²/g capacitance up to 4000 F/g could be reached in an electrode

If max Voltage = 1V the Energy density $E = 35 \text{ W}\cdot\text{h}/\text{kg}$; if 3V, $E=315 \text{ W}\cdot\text{h}/\text{kg}$

2. Semi-empirical estimation:

Assume formation of a close-packed monolayer of solvated ions (1e; d = 1.5 nm): 0.4 C/m²

If could be achieved @ 1V: Capacitance = 4,000 uF/cm² and $E = 1,400 \text{ W}\cdot\text{h}/\text{kg}$

If could be achieved @ 10V: Capacitance = 400 uF/cm² and $E = 14,000 \text{ W}\cdot\text{h}/\text{kg}$

3. Fundamental limit:

If 1e/atom in electrode: eNV/2 per electrode (1/2 of batteries **but** V_{supercap} could be >2x higher)

Will micro-fabrication affect supercapacitor performance ?

- Power achievable is related to the Equivalent Series Resistance (ESR)

$$ESR = R_{cc/electrode} + R_{electrode} + R_{electrolyte} + R_{separator}$$

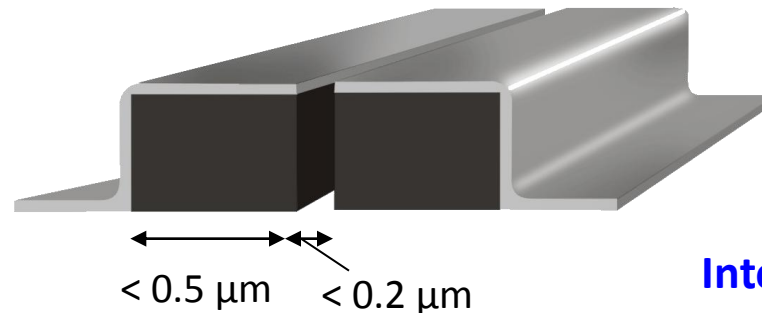
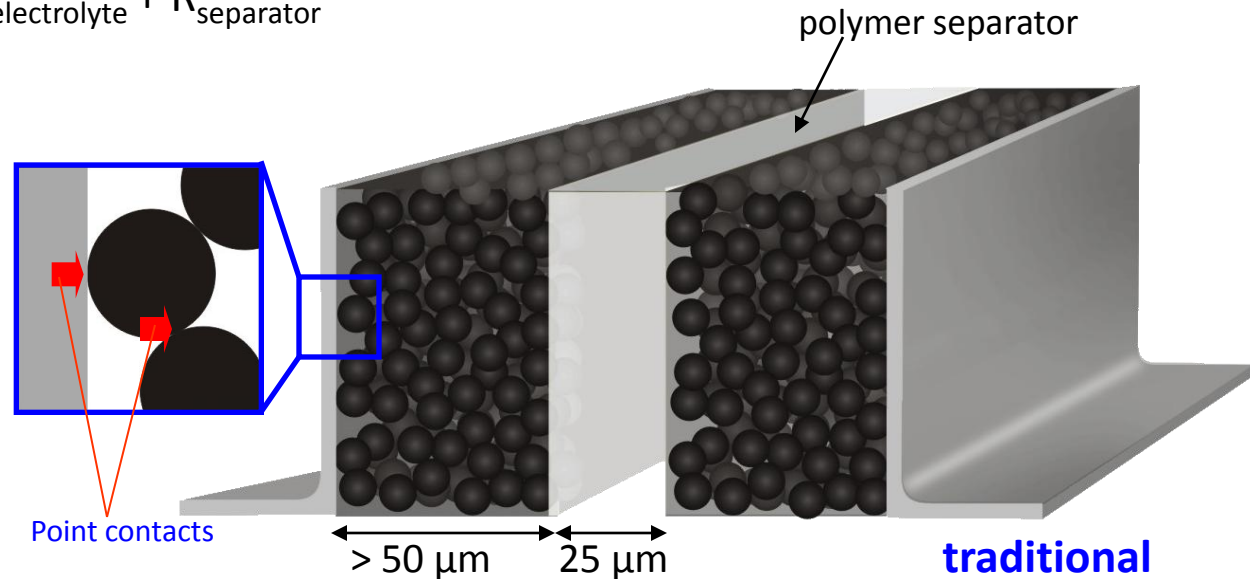
By moving from traditional to integrated supracapacitor we:

- decrease $R_{cc/electrode}$ by >100
- decrease $R_{electrode}$ by >100
- decrease $R_{electrolyte}$ by >100
- decrease $R_{separator}$ by >100



Integrated supercap:

- $> 100x$ Power_(gravimetric)
- $> 200x$ Power_(volumetric)
- $< 1\%$ Charging time ($t_{diff} \sim x^2$)



IV. Supercapacitors

Double Layer Capacitors

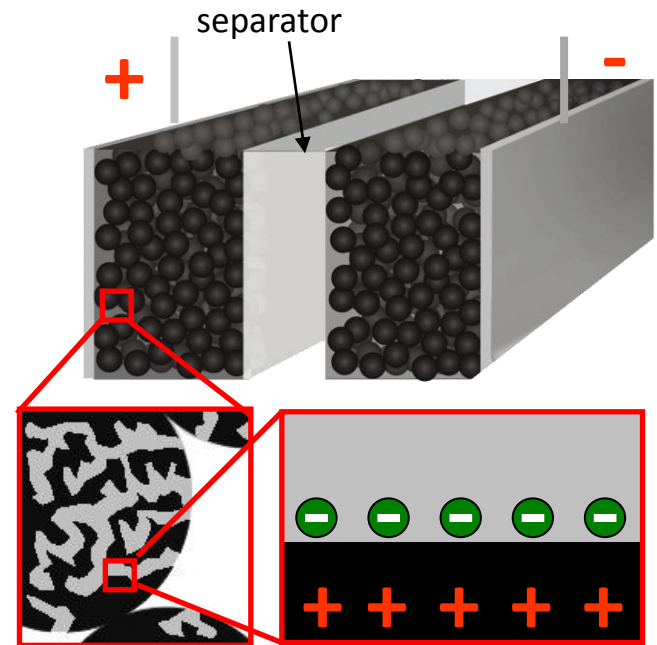
$$E = \frac{CV^2}{2}; P \approx \frac{E}{\tau}$$

E - energy; P - power; C - capacitance; τ - discharge time

$$C = \frac{Q}{V} = \epsilon_0 \epsilon_r \frac{A}{d} \text{ (Farads)}$$

C - capacitance; Q - charge; A - area;

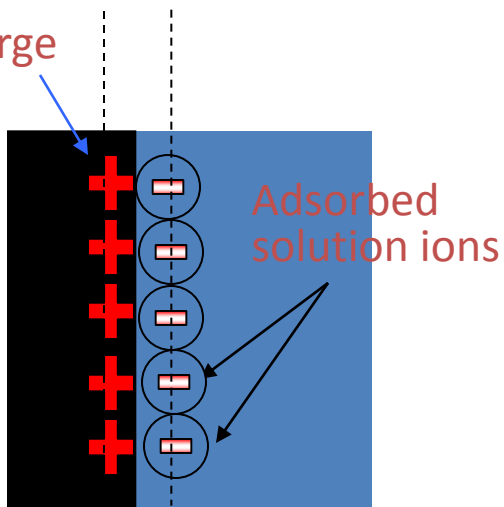
d - separation distance between the ions and pore walls



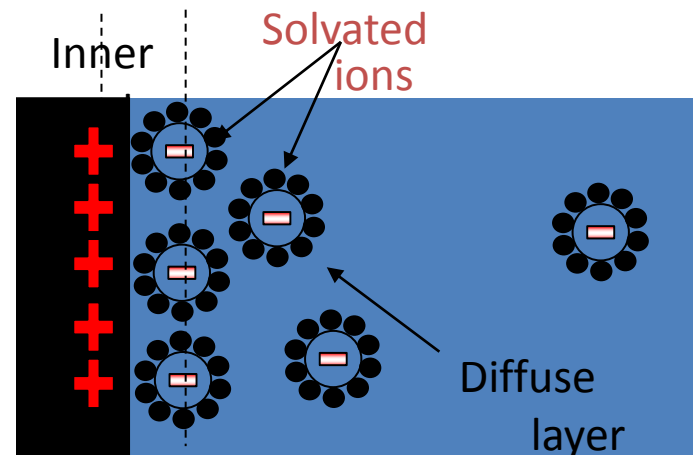
Helmholtz Model

Surface charge

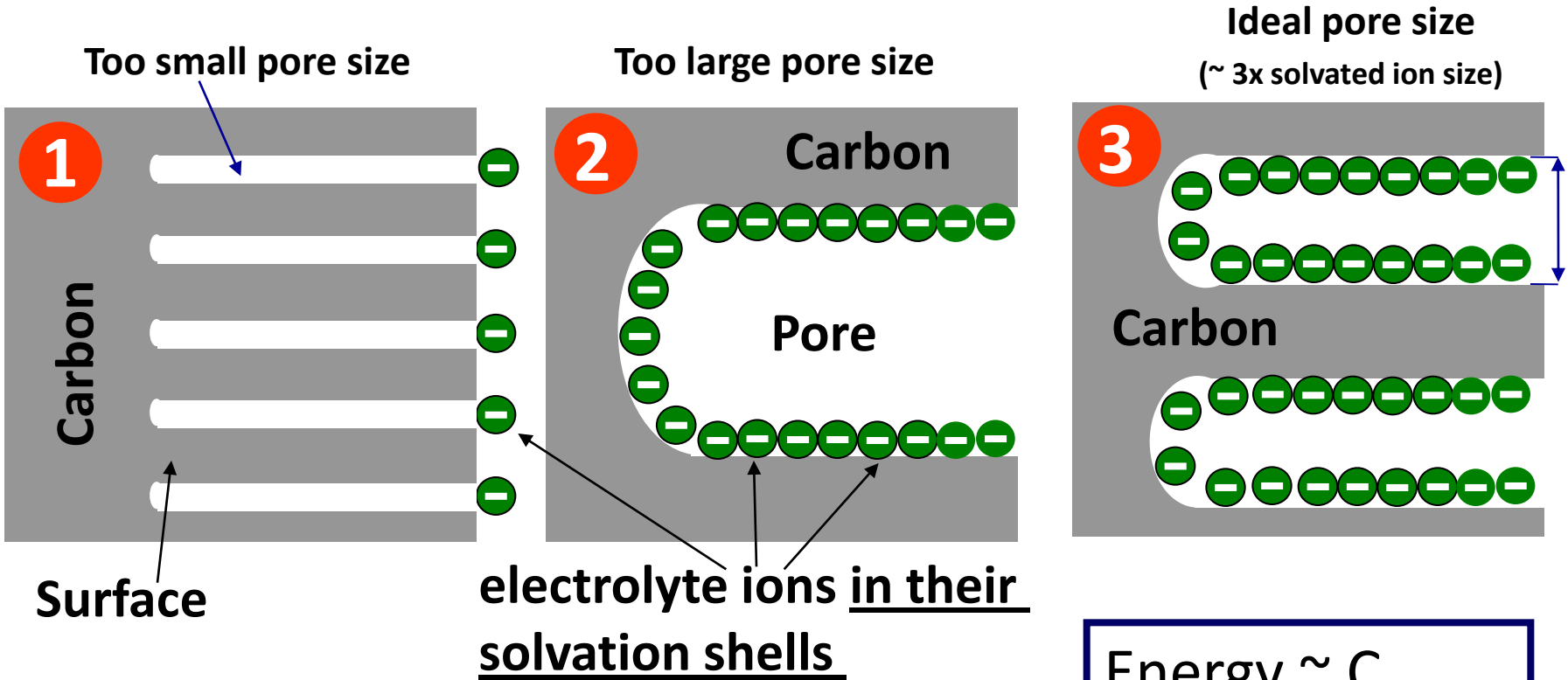
Positively charged electrode (+V)



Gouy-Chapman-Stern Model



Double Layer Capacitors: Effect of Pore Size on Capacity (Energy)



Traditional view

$$\text{Energy} \sim C$$
$$\text{Power} \sim \sqrt{\frac{C}{R}}$$

Supercapacitors – R&D Status

- High Energy Density / High Frequency (100-1000 Hz) operation has never been demonstrated
- Intergated Supercaps never demonstrated
- Solid Electrolyte operating at high frequency – a challenge
- Experimental data on the effects of various parameters on ion transport in thin films are very limited
- Experimental data on the electrical resistance of the electrodes and interfaces are very limited

Planar and Integrated Supercapacitors

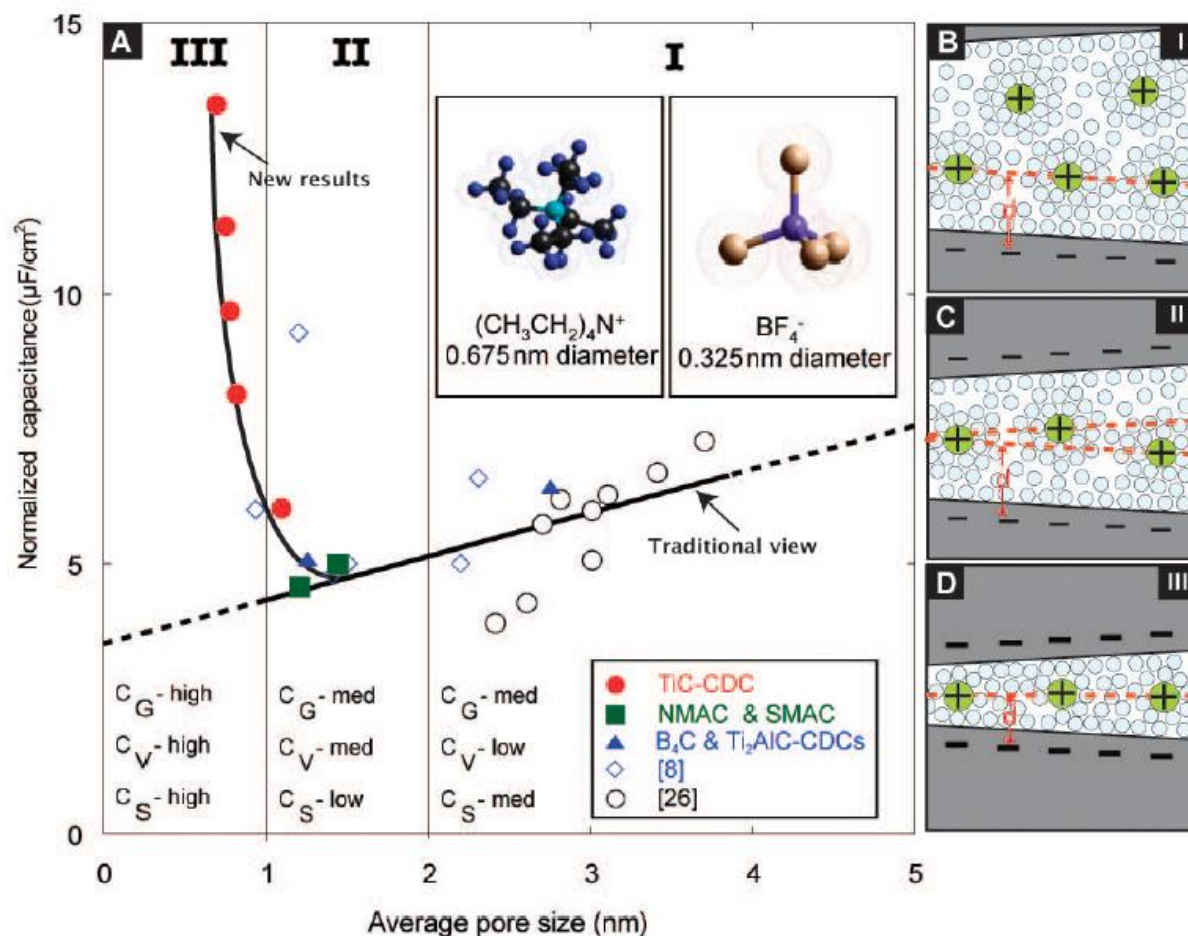
Objectives:

- Thin film or planar components to enhance the energy and power densities for efficient power supply, conversion and regulation.
- Optimization of geometry / architecture for controlled Energy/Rate performance
- Planar supercapacitor components for easier integration in the packaging

Proposed R&D

- Patterned deposition of either CNT (or metal nanowires) on Si wafer surface via CVD
- Surface coating with metal oxide layer (via ALD or CVD)
- Developing successful process flows for the formation of integrated devices based on the proposed architecture
- Studying effects of film thickness, porosity, architecture and metal oxide microstructure on the frequency response, capacitance and power characteristics
- Developing new routes for infiltration of electrodes with polymer electrolyte and investigate the effects of electrolyte (polymer, solvent, salt) on frequency response

Double Layer Capacitors: Effect of Pore Size on Capacity

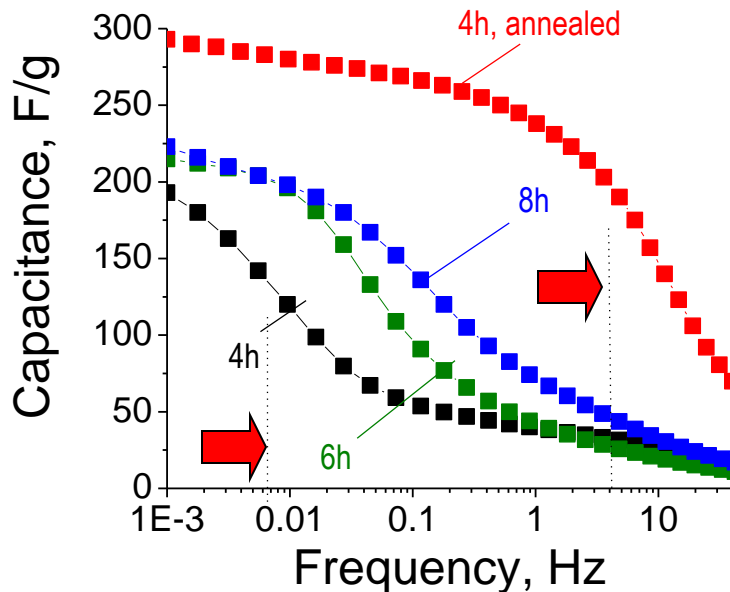
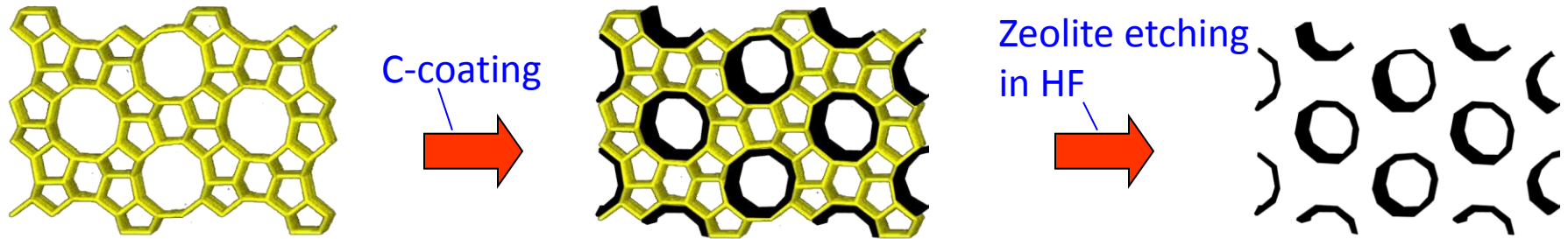


➤ Distortion of solvation shells in sub-nm pores results in enhanced ion storage capacities

➤ $C \sim 1/d$

Double Layer Capacitors: Effect of Pore Alignment on the Rate of Ion Transport (Power)

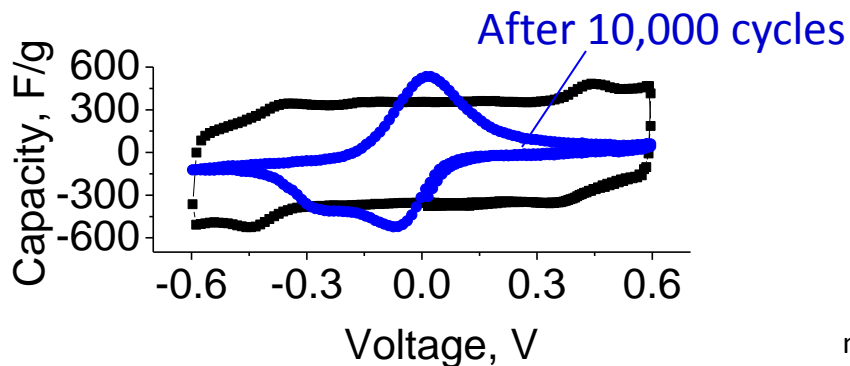
- Employed zeolites as sacrificial templates (as originally proposed by Kyotani)



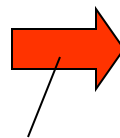
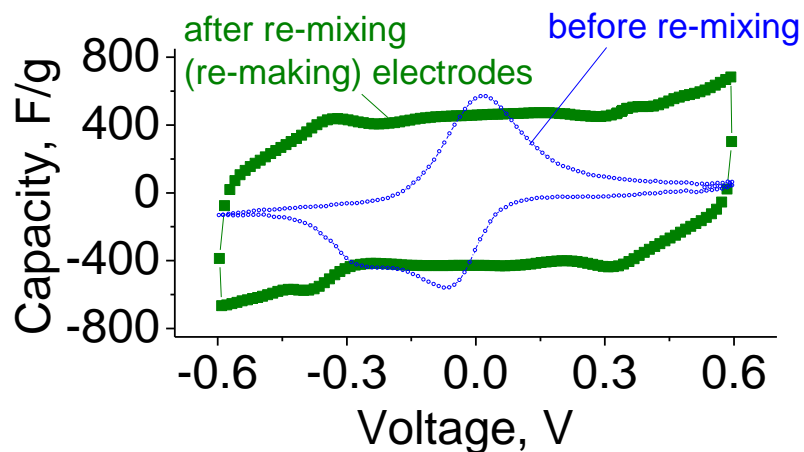
Frequency response of EDLC based on 0.3 mm thick electrodes as a function of pore alignment: aligning the pores allowed nearly 3 orders of magnitude faster ion transport rate in 1 nm pores (and thus 3 orders of magnitude higher power)

Pseudo-Capacitors: Polymer-Based (Solution Processing Possible)

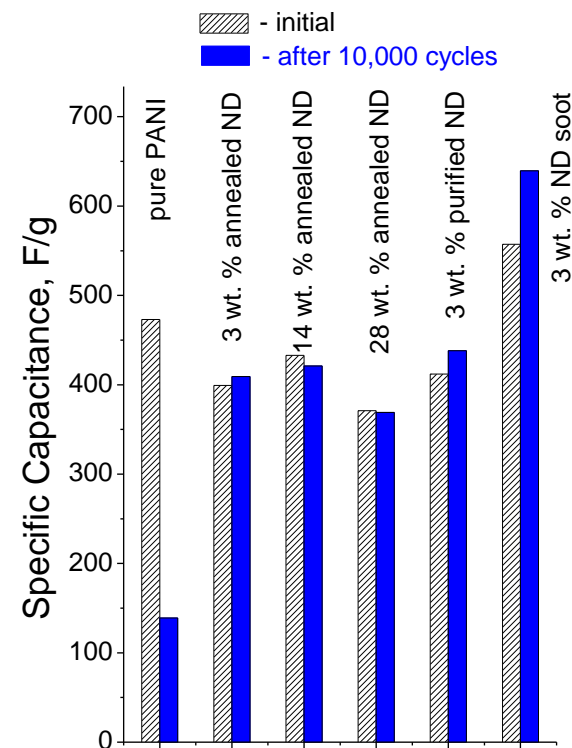
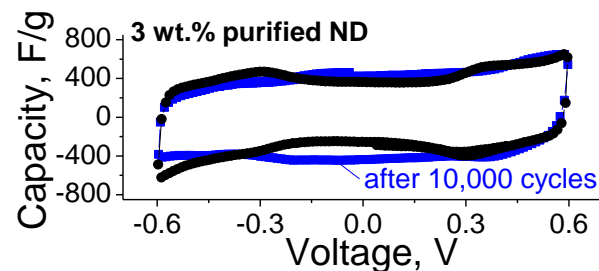
Regular PANI



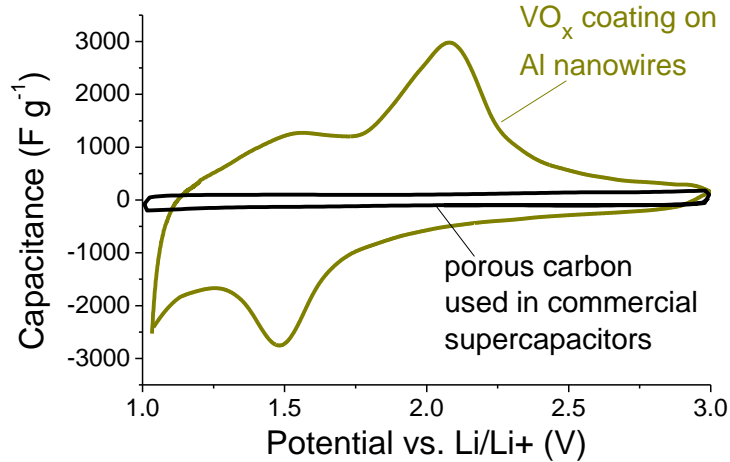
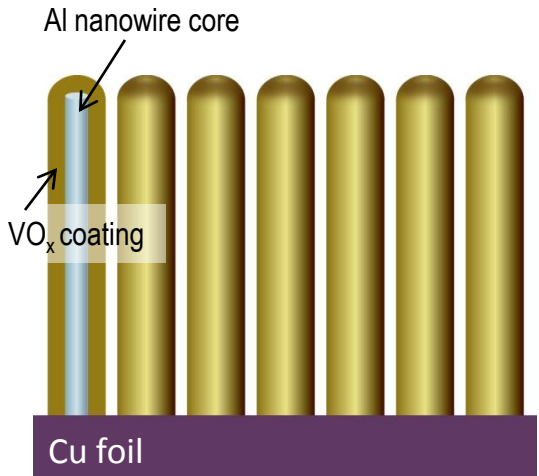
pure PANI after 10,000 cycles



By incorporating nanopowder (e.g., nanodiamond powder) into PANI and by controlling NP-pani interactions, greatly enhanced stability could be achieved

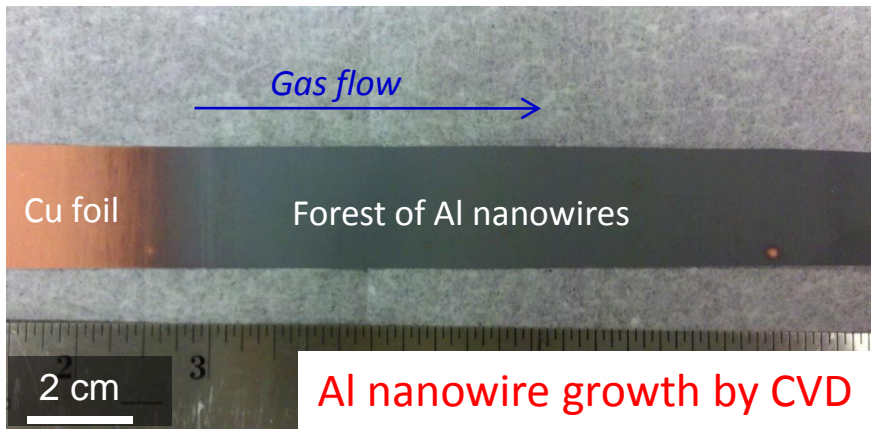


Pseudo-Capacitors: Transition Metal Oxide Coatings on Carbon Nanotubes or Metal Nanowires via Vapor Deposition (CVD or ALD)

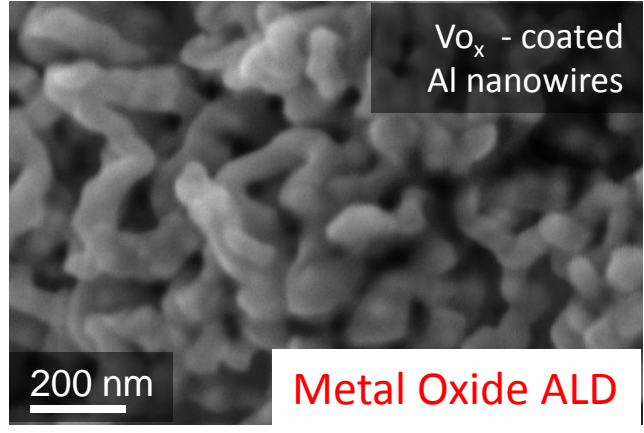


➤ Transition Metal oxide provides high capacitance but suffers from low electrical conductivity

➤ Metal Nanowires provide highly conductive high surface area support



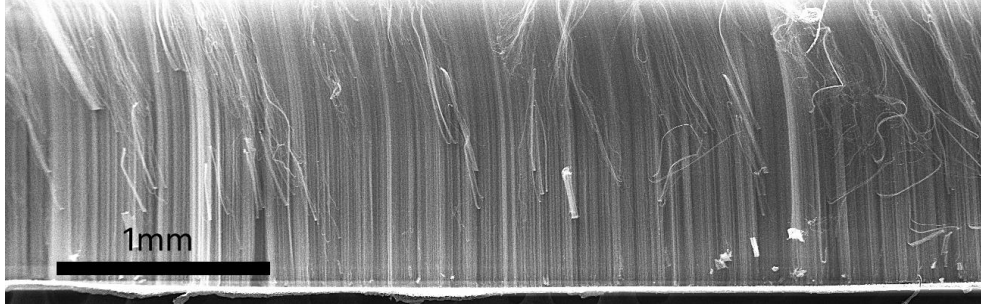
Al nanowire growth by CVD



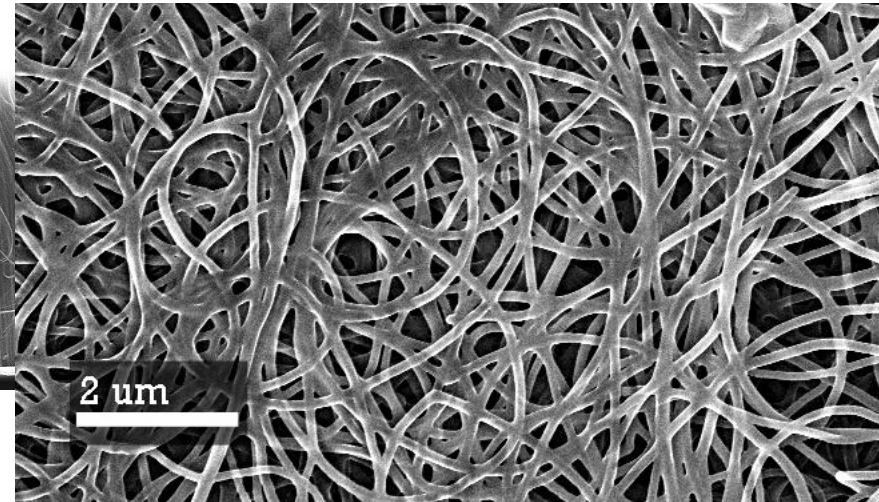
Metal Oxide ALD

Pseudo-Capacitors: Transition Metal Oxide Coatings on Carbon Nanotubes or Metal Nanowires via Vapor Deposition

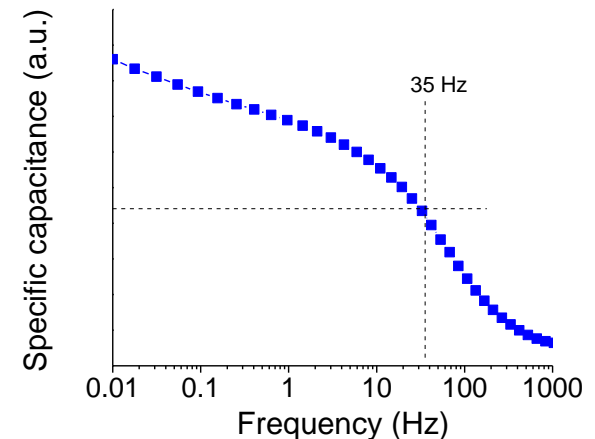
Aligned CNT on a current collector



Misaligned V_xO -CNT electrode



- CNT growth is faster than that of metal nanowires
- However, higher temperatures are needed (without plasma enhancement) and the interface between CNT and metal oxide could be inferior



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