

Georgia Tech PRC - ECTC 2011 Abstracts

TITLE	ABSTRACT
<p>Chip-Package Electrical Interaction in Organic Packages with Embedded Actives</p> <p>Nithya Sankaran, Hunter Chan, Madhavan Swaminathan, Venky Sundaram, Rao Tummala, Telesphor Kamgaing and Vijay.K.Nair</p>	<p>System integration and miniaturization needs are the driving factors for embedding active and passive components within packages. But embedding components also results in unwanted interferences within the package. This paper demonstrates chip-package interaction in the form of electromagnetic interference between the embedded chip and its package. The electromagnetic coupling experienced by the bond-pads of the embedded chip, the effect of bulk substrate of the embedded chip on the coupling across the package and the influence of die to cavity clearance on the vertical electromagnetic coupling across the different layers of the package housing the embedded chip are analyzed. Results from simulations and measurements are presented to demonstrate the phenomena studied.</p> <p>For additional information, please contact: Dr. Venky Sundaram at vs24@mail.gatech.edu</p>
<p>Conformal Atomic Layer Deposition (ALD) of Alumina on High Surface-Area Porous Copper Electrodes to Achieve Ultra-High Capacitance Density on Silicon Interposers</p> <p>Kanika Sethi, Himani Sharma, P. Markondeya Raj, Venky Sundaram, Rao Tummala</p>	<p>Abstract</p> <p>This paper describes an innovative approach to achieve higher capacitance density on silicon interposers than what has been reported with trench capacitors. The approach consists of a novel silicon-compatible low-temperature sinterable metal particulate electrode and a conformal moderate K dielectric to attain the high volumetric efficiencies. The nanoparticle electrodes lead to much higher area enhancement compared to planar or trench structures resulting in ultrahigh capacitance densities. Copper nanoparticles were directly sintered on silicon substrates to form high surface area electrodes with engineered porosity. These high surface area copper electrodes were conformally- coated with moderate- permittivity dielectrics using Atomic Layer Deposition (ALD). Combination of compositional and morphological techniques, EDS and SEM respectively, were used to show alumina conformality on complex 3-D structures of copper particulate electrodes. I-V and C-V characterization was performed to confirm the feasibility of the novel high density 3-D capacitor structure. Capacitance densities of 30 $\mu\text{F}/\text{cm}^2$ at high voltages have been demonstrated with this approach.</p> <p>For additional information, please contact: Dr. P.M. Raj at raj.pulugurtha@ece.gatech.edu</p>
<p>Co-W as an Advanced Barrier for Intermetallics and Electromigration in Fine-Pitch Flipchip Interconnections</p> <p>Dibyajat Mishra, P. Markondeya Raj, Sadia Khan, Nitesh Kumbhat, Yushu Wang, Suman Addya Raghuram V Pucha, Abhishek Choudhury, Venky Sundaram and Rao Tummala</p>	<p>The trend towards thinner packages with embedded active components in case of RF modules, and higher I/O densities in case of multicore processors or 3D ICs, are pushing interconnection technologies to its fundamental limits. The limitations of traditional solder bump technologies in terms of its fatigue resistance, current-handling, electromigration and thermomigration resistance has shifted the interconnection focus to advanced thick copper bump UBMs with solder caps. However, even these interconnections fail to meet thermo-mechanical and electrical reliability requirements for fine-pitch flipchip interconnections at high current densities where electromigration becomes a major concern. This paper explores Co-W as an advanced barrier between copper bump and solder cap for fine-pitch flipchip technology to improve electromigration resistance. By suppressing the intermetallic growth and controlling electromigration, the novel barrier is expected to enhance the current-handling and thermomechanical reliability. In a systematic experimental study, Cu-Sn diffusion and intermetallic growth rate of this new Cu--Co-W--Sn-Ag approach are compared with that of Cu--Sn-Ag with XPS depth-profiling and</p>

	<p>cross-section analysis using SEM and EDS. Based on the analysis, the benefits of Co-W as a solder barrier for fine-pitch flipchip interconnections at high current densities is presented.</p> <p>For additional information, please contact: Dr. P.M. Raj at raj.pulugurtha@ece.gatech.edu</p>
<p>Design and Demonstration of Low Cost, Panel-based Polycrystalline Silicon Interposer with Through-Package-Vias (TPVs)</p> <p>Qiao Chen, Tapobrata Bandyopadhyay, Yuya Suzuki, Fuhun Liu, Venky Sundaram, Raghuram Pucha, Madhavan Swaminathan, and Rao Tummala</p>	<p>This paper for the first time proposes and demonstrates the use of panel-based polycrystalline silicon interposers for highest I/Os at lowest cost. Such an interposer is targeted at roughly a 10x lower cost compared to wafer based silicon interposers with through silicon vias (TSVs) and back end of line (BEOL) re-distribution layers (RDL). Laser via ablation was used to demonstrate through package vias (TPVs) as small as 10μm diameter in 220μm thin polycrystalline silicon panels made without any chemical-mechanical polishing (CMP). A thick polymer via liner and stress buffer layer was formed in the silicon TPVs to replace oxide liners and diffusion barriers used in TSVs. A panel silicon interposer test vehicle process demonstrator was fabricated and initial electrical measurements indicate much lower loss compared to CMOS silicon interposer with thin oxide liners. Electrical and mechanical design and modeling was also carried out to provide design guidelines for TPV formation.</p> <p>For additional information, please contact: Dr. Venky Sundaram at vs24@mail.gatech.edu</p>
<p>Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through-Package-Vias</p> <p>Vijay Sukumaran, Tapobrata Bandyopadhyay, Qiao Chen, Nitesh Kumbhat, Fuhun Liu, Raghu Pucha, Yoichiro Sato[^], Mitsuru Watanabe, Kenji Kitaoka, Motoshi Ono, Yuya Suzuki, Choukri Karoui, Christian Nopper, Madhavan Swaminathan, Venky Sundaram and Rao Tummala</p>	<p>Abstract</p> <p>This paper demonstrates thin glass interposers with fine pitch through package vias (TPV) as a low cost and high I/O substrate for 3D integration. Interposers for packaging of ULK and 3D-ICs need to support large numbers of die to die interconnections with I/O pitch below 50 μm. Current organic substrates are limited by CTE mismatch, wiring density, and poor dimensional stability. Wafer based silicon interposers can achieve high I/Os at fine pitch, but are limited by high cost. Glass is an ideal interposer material due to its insulating property, large panel availability and CTE match to silicon. The main focus of this work is on a) electrical and mechanical design, b) TPV and fine line formation and c) integration process and electrical characterization of thin glass interposers. This work for the first time demonstrates high throughput formation of 30 μm pitch TPVs in ultrathin glass using a parallel laser process. An integration process was demonstrated for glass interposer with polymer build-up layers on both sides. The glass interposer had stable electrical properties up to 20GHz and low insertion loss of less than 0.15dB was measured for TPVs at 9GHz.</p> <p>For additional information, please contact: Mr. Nitesh Kumbhat at nitesh@ece.gatech.edu</p>
<p>High Density Electrical Interconnections in Liquid Crystal Polymer (LCP) Substrates for Retinal and Neural Prosthesis Applications</p> <p>Venky Sundaram, Vijay Sukumaran, Michael E. Cato, Fuhun Liu, Rao Tummala Patrick J. Nasiatka, James D. Weiland, and Armand R. Tanguay, Jr.</p>	<p>Retinal prostheses implemented by means of electrical stimulation of retinal ganglion cells have been previously demonstrated with 16 and 60 channel microstimulator arrays. Blind patients with severe retinal degeneration (e.g., retinitis pigmentosa (RP) have been able to use these devices to navigate and read large letters. However, to dramatically improve the effectiveness of such prostheses, and to enable a variety of neural stimulation implants, channel densities of 1000 per cm² and higher are highly desirable. This paper reports on a novel approach to an integrated bioelectronic package with high density electrical feedthroughs, capable of 1024 stimulator channels in a 5 mm \times 5 mm area using liquid crystal polymer (LCP) substrates to enable implantable retinal prostheses. A novel fusion bonding process was demonstrated to achieve fine pitch interconnections with high adhesion strength and biocompatible metal-</p>

	<p>polymer interfaces. Helium leak rates of 1×10^{-9} mbar-l/sec were measured for LCP samples without feedthroughs, representative of penetration through the bulk LCP film, and leak rates of $< 5 \times 10^{-8}$ mbar-l/sec were measured for feedthrough array samples, comparable to leak rates demonstrated for glass substrates with metallized vias.</p> <p>For additional information, please contact: Dr. Venky Sundaram at vs24@mail.gatech.edu</p>
<p>High Throughput and Fine Pitch Cu-Cu Interconnection Technology for Multichip Chip-Last Embedding</p> <p>Abhishek Choudhury, Nitesh Kumbhat, Sadia A Khan, P. Markondeya Raj, Venky Sundaram, Georg Meyer-Berg and Rao Tummala</p>	<p>Ultra-thin packages with embedded actives for high functional density have become strategically important with fast growing market for portable electronics. 3D Packaging Research Center at Georgia Tech is pioneering a chip-last approach for die embedding using adhesively bonded copper bumps to enable ultra-fine pitch chip-to-package interconnections. This paper presents three advancements over the adhesive bonding technology demonstrated previously- 1) A novel method to perform chip-last at panel-level, leading to 10-15x reduction in assembly time per die, 2) Improved 2-step assembly process to achieve simultaneous die embedding and cavity planarization, and 3) Adhesive bonding of high I/O die. To demonstrate high throughput assembly, x-ray and electrical yield results for an 8-10 dies, simultaneously bonded on a 3" x 3" panel with high accuracy have been discussed. The assembly process modification yielded planarization of the gap between the die and cavity wall to $< 1\mu\text{m}$. Electrical yield of adhesively bonded large die with ~ 800 I/Os has also been discussed. These technology advancements aim to address some of the key limitations of conventional adhesive based assemblies, thus making chip-last adhesive bonding with low profile copper-to-copper interconnections a robust chip embedding solution for next-generation of highly integrated heterogeneous subsystems.</p> <p>For additional information, please contact: Mr. Nitesh Kumbhat at nitesh@ece.gatech.edu</p>
<p>Low cost, Chip-Last Embedded ICs in Thin Organic Cores</p> <p>Nitesh Kumbhat, Fuhan Liu, Venky Sundaram, Georg Meyer-Berg, and Rao Tummala</p>	<p>This paper presents a novel technology to enable chip embedding in 1 or 2 metal layer substrates using chip-last embedding for its merits. The novel structure is obtained by embedding thin-chips within the core instead of the build-up layers as has been demonstrated previously [1]. To enable the smallest profile embedded die structure, results from the three critical elements of the technology- 1) fine lines and spaces on core, 2) small-diameter fine-pitch area-array through-holes, and 3) thermo-mechanical reliability of small diameter through-holes have been discussed in the paper. Lines and spaces as small as $7\mu\text{m}$ were demonstrated on core laminate by using build-up type processes. Copper-filled through-holes of 30-60μm diameters were successfully fabricated and shown to pass 1300 thermal cycles from -55°C to 125°C. In addition, through-hole drilling process was optimized to achieve ultra-fine pitches of 70-100μm.</p> <p>Comprehensive analysis of three new materials and associated fabrication processes, carried out to demonstrate the advantages and robustness of this manufacturing-friendly 1-2 metal layer chip-last embedding technology emphasizes that it is a promising technology to achieve ultra-miniaturization for future embedded systems and sub-systems.</p> <p>For additional information, please contact: Mr. Nitesh Kumbhat at nitesh@ece.gatech.edu</p>
<p>Novel Nanomagnetic Materials for High-Frequency RF Applications</p>	<p>This paper describes leading-edge research to explore and demonstrate new and unique nanoscale magnetic composites for high-frequency RF applications. Passivated cobalt nanoparticles were chemically synthesized and dispersed in</p>

<p>P Markondeya Raj, Himani Sharma, G. Prashant Reddy, David Reid, Nevin Altunyurt, Madhavan Swaminathan and Rao Tummala</p>	<p>epoxy to fabricate nanocomposite thick films. The high permeability comes from enhanced coupling between the metal nanoparticles while the insulating polymer matrix prevents eddy current loss and improves stability with frequency. Test vehicles were fabricated to demonstrate integration of these composites in organic substrates and to characterize the high-frequency properties.</p> <p>The frequency-dependent magnetic properties in 100-500 MHz range were extracted by impedance spectroscopy. Magnetic toroids were mechanically pressed with the metal-insulator powder. By refining the processing, permeability of 2.7 was demonstrated at VHF frequencies. The loss tangent was less than 0.04 at these frequencies.</p> <p>The GHz frequency-dependent material characteristics of the magneto-dielectric films were extracted from corner-probing of parallel-plate resonators and strip inductors. By engineering the composite structures at nanoscale, a combination of stable permeability of ~ 2 at 1-5 GHz and permittivity of 7, not previously reported, was achieved with polymer composites for antenna miniaturization. The magnetic nanomaterials with low loss, described in this paper, can benefit several other RF and power components, leading to their miniaturization and performance enhancement in emerging RF sub-systems. The metal composite structures also lead to high permittivity in the GHz frequencies which can benefit such RF components as antennas, by allowing closer impedance matching with air.</p> <p>For additional information, please contact: Dr. P.M. Raj at raj.pulugurtha@ece.gatech.edu</p>
<p>Reliability of Fine Pitch Halogen-Free Organic Substrates for Green Electronics</p> <p>Koushik Ramachandran, Fuhan Liu, Nitesh Kumbhat, Mark Wilson, Venky Sundaram, and Rao Tummala</p>	<p>Abstract European Union's Regulation on halogens and lead-based solders has lead to the development of new class of high Tg halogen-free polymer-glass laminates for package substrates. At the same time, Moore's law and 3D ICs have accelerated the demand for high I/O density. These fine pitch requirements in new substrates can affect reliability in terms of loss of surface insulation resistance (SIR) and formation of conductive anodic filament (CAF) leading to electrical failures. Therefore newly developed materials are required to have excellent resistance to electrochemical migration and high thermal stability for lead-free assembly. This study focuses on experimental reliability study of novel halogen-free substrates under accelerated conditions. This study consists of 1) SIR test with 50 μm line width/spacing, 2) CAF test of through-vias of 100 μm diameter with pitch of 250 μm and 500 μm, 3) through-via reliability and, 4) Pb-free flip-chip package reliability with halogen-free substrates. The halogen-free substrate used in this work was observed to have high resistance to surface migration at 50 μm line-width/ spacing. However, CAF failures were observed even at 250 μm pitch indicating that failures due to CAF at fine pitch are a serious reliability concern. The substrates did not show any failures in through-vias and flip-chip interconnections under thermal cycling indicating good reliability for halogen-free and Pb-free applications.</p> <p>For additional information, please contact: Mr. Nitesh Kumbhat at nitesh@ece.gatech.edu</p>
<p>Solution-Derived Electrodes and Dielectrics for Low-Cost and High-Capacitance Trench and Through-Silicon-Via (TSV) Capacitors</p>	<p>This paper explores and demonstrates a novel technique to conformally coat solution-derived electrodes and dielectric films over Through-Silicon-Via (TSV) or Through-Silicon Trench (TST) structures. In this technique, precursor solution for electrode or dielectric coatings is dispensed on the top of a TSV wafer and infiltrated through the via by creating a pressure gradient. Two material systems</p>

<p>Yushu Wang, Shu Xiang, P. Markondeya Raj, Himani Sharmaa, Byron Williams and Rao Tummala</p>	<p>used in capacitors, Lanthanum Nickel Oxide (LNO) as electrode and Lead Zirconate Titanate (PZT) as dielectric, were deposited on the TSV surfaces using this technique. SEM cross-section analysis showed that the vacuum-infiltration can be extended to conformally coat on trenches with aspect ratios of greater than 5. A planar capacitor with density of 3 $\mu\text{F}/\text{cm}^2$ and low leakage was fabricated to demonstrate the material compatibility. Using this technique, a trench capacitor device can be fabricated with an all-solution coating process, without involving any expensive deposition tools. This can thus eliminate costly platinum electrodes that are frequently required to yield high permittivity PZT films. This technique can also address the through-put limitations of today's conformal deposition technologies such as sputtering, Chemical Vapor Deposition (CVD) and Atomic Layer Deposition (ALD). The tool and process can also be applied to other 3D silicon structures where conformal ceramic coatings are needed.</p> <p>For additional information, please contact: Dr. P.M. Raj at raj.pulugurtha@ece.gatech.edu</p>
<p>Thermo-Mechanical Behavior of Through Silicon Vias in a 3D Integrated Package with Inter-Chip Microbumps</p> <p>Xi Liu, Qiao Chen, Venkatesh Sundaram, Margaret Simmons-Matthews, Kurt P. Wachtler, Rao R. Tummala, and Suresh K. Sitaraman</p>	<p>Through-silicon via (TSV), being one of the key enabling technologies for 3D system integration, is being used to interconnect 3D vertically stacked devices, such as logic, memory, sensors, and actuators that are fabricated on separate wafers and then interconnected by either wafer-to-wafer or chip-to-wafer methods. However, thermo-mechanical analyses on TSVs are limited, and most of the existing studies focus on the thermo-mechanical analysis of TSVs in a free-standing wafer, rather than in an integrated package.</p> <p>In this paper, three-dimensional thermo-mechanical finite-element models have been built to analyze the stress/strain distribution in a 3D integrated package which contains stacked dice with TSVs, inter-chip microbumps, overmold, and underfilled solder bumps, and an organic substrate. Models show that the stresses in the TSV under packaging configuration could be generally lower than the stresses in the TSV in a free-standing wafer. Also, the models show that the high-strain region switches from TSV corners to microbumps.</p> <p>For additional information, please contact: Dr. Venky Sundaram at vs24@mail.gatech.edu</p>
<p>Ultra-high I/O Density Glass/Silicon Interposers for High Bandwidth Smart Mobile Applications</p> <p>Gokul Kumar, Tapobrata Bandyopadhyay, Vijay Sukumaran, Venky Sundaram, Sung Kyu Lim and Rao Tummala</p>	<p>Smart mobile applications are driving the demand for higher logic-to-memory bandwidth (BW) in 10-30GB/s range with lower power consumption and larger memory capacity. This paper presents a radically-different, scalable and lower cost approach than the 3DICs with TSV stack approach being pursued widely, to achieve high bandwidth. This approach is referred to as interposer approach using ultra-thin glass or silicon with ultra-high I/O density interposers, which does not require TSVs in the logic IC in the 3D stack. This paper presents a comparative study, based on electrical modeling of the logic-to-memory signal path, in various current and emerging package configurations for use in smart mobile devices. Frequency and time domain analysis for each of these scenarios is performed using both chip and package-level models with varying interconnection dimensions. Simulated eye diagrams for the complete data paths in the thin glass interposer approach demonstrated more than 3Gbps/pin data rate, similar to 3DICs.</p> <p>For additional information, please contact: Dr. Venky Sundaram at vs24@mail.gatech.edu</p>
<p>Ultra-Miniaturized WLAN RF</p>	<p>The first demonstration of an ultra-miniaturized WLAN (2.4 GHz) receiver module</p>

<p>Receiver with Chip-Last GaAs Embedded Active</p> <p>Vivek Sridharan, Abhilash Goyal, Srikrishna Sitaraman, Nitesh Kumbhat, Nithya Sankaran, Hunter Chan, Fuhan Liu, Debasis Dawn, Vijay Nair, Telesphor Kamgaing, Frank Juskey, Venky Sundaram, and Rao Tummala</p>	<p>with chip-last Embedded Actives (Low Noise Amplifier) and Embedded Passives (low pass filter) is presented. The 100μm thick low noise amplifier (LNA) GaAs dies were embedded in an ultra-thin, low loss organic package substrate in close proximity to an embedded RF filter. The low pass filter had an insertion loss of less than 0.3 dB and return loss better than 20dB at 2.4 GHz. The measured gain of the LNA Module was 13.22 dB with a noise figure of 1.7 dB. The overall thickness of the package including embedded ICs was 300μm resulting in significant z-height reduction compared to current wire bond and flip chip packages. Chip-last embedding enables testability of ICs and embedded passives substrate prior to chip embedding for high yield.</p> <p>For additional information, please contact: Mr. Nitesh Kumbhat at nitesh@ece.gatech.edu</p>
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