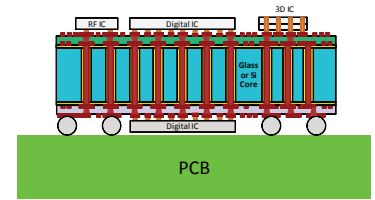


Low-Cost, Panel Based Glass and Silicon Packages Consortium

Georgia Tech 3D Systems Packaging Research Center (PRC) invites companies to join its Global Industry Consortium in low cost and high I/O silicon and glass packages for 2D and 3D ICs.



What

- Panel-based glass and silicon packages with 20-50 μ m pitch to interconnect 3D ICs at \sim 10x lower cost than wafer-based silicon interposers

Why

- 3D ICs need packages with very high I/Os at very small pitch and at very low cost
- Si interposers address this need but are expected to be too expensive on cost per I/O basis
- Organic packages are reaching limits in I/O density, thermal and cost per I/O

Georgia Tech PRC Proposal

Georgia Tech proposes panel-based glass and silicon packages to address the above by:

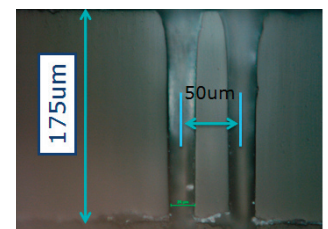
- Demonstration of \sim 5x improvement in I/O density at \sim 10x lower cost
- Addressing two major barriers: 1) low cost TPVs and 2) improved thermal conductivity
- Extending these packages with minimum re-distribution layers to add embedded thin-film components, and SMT reliability to organic boards

The Unique Features of this Global Consortium Include:

- Focus on low cost high I/O packages – 8x reduction from larger panels, 2x reduction from package materials and processes
- Address fundamental barriers to use of glass – form TPV holes at much lower cost than TSV, and improve its thermal conductivity
- Develop high throughput processes for vias, wiring and interconnections
- Focus on high interconnection reliability and high yield
- Develop both panel and wafer-compatible processes
- Clear path to commercialization through key IDM and supply chain partners

Research Focus

- Electrical and thermo-mechanical design
- Ultra-thin, large-area and low-cost silicon and glass core materials
- Low-cost through-package-via (TPV) materials and processes
- Low-cost and high I/O double-sided interconnections
- Package to PWB Interconnection materials and processes and reliability
- Thermal conductivity improvements
- Embedded thin film components



Glass and Silicon Packages Research Tasks and Team

Dr. Venky Sundaram (Program Manager)

- Thin Substrates and Cavities – Dr. Fuhan Liu, Mr. Hunter Chan
- Electrical & Mechanical Design – Mr. Tapo Bandyopadhyay, Mr. Vivek Sridharan, Mr. Qiao Chen, Mr. Nitesh Kumbhat, Dr. Raghu Pucha
- TPV in Glass and Silicon – Mr. Vijay Sukumaran, Mr. Qiao Chen
- High I/O Wiring – Dr. Fuhan Liu, Mr. Hunter Chan, Mr. Vivek Sridharan, Mr. Vijay Sukumaran, Mr. Qiao Chen
- IC-Package-PWB Interconnections – Mr. Nitesh Kumbhat, Dr. Raj Pulugurtha
- Embedded Components – Dr. Raj Pulugurtha, Dr. Himani Sharma, Mr. Vivek Sridharan
- Thermal Management – Prof. Yogendra Joshi, Dr. Raj Pulugurtha
- Demonstrator – Mr. Vijay Sukumaran, Mr. Qiao Chen, Mr. Tapo Bandyopadhyay, Mr. Vivek Sridharan, Mr. Hunter Chan, Dr. Venky Sundaram, Mr. Nitesh Kumbhat, Dr. Fuhan Liu
- Industry Liaison and Memberships – Mr. Dean Sutter, Director of Operations
- Professor Rao Tummala (PRC Director)

Website:

www.prc.gatech.edu/
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