

# Abhilash Goyal

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## Objective

Full time opportunity to contribute in exciting and challenging area in the field of electronics. My PhD research primarily focuses on packaging including RF/Mixed-signal design and test. I am open to new opportunities as well

## Education

### Georgia Institute of Technology, Atlanta, Georgia, USA

- 2006 - Present      Ph.D candidate in School of Electrical and Computer Engineering  
*Research area:* RF/Mixed-Signal Package Design, Testing and Modeling.  
*Advisor:* Prof. Swaminathan, Madhavan
- April 2010          *Certified in Microsystems Packaging* from 3D Systems Packaging Research Centre
- 2005 – 2006        Master's in Electrical and Computer Engineering  
Major *GPA:* 4.0/4.0

### Indian Institute of Technology (IIT), Kharagpur, West Bengal, India

- 1998 – 2002        Bachelor of Technology (Honors) , Electronics and Electrical Communication Engineering  
Major *GPA:* 8.77/ 10.00

## Georgia Institute of Technology, Atlanta, USA

### Graduate Studies

#### *Research and projects*

- Working on the development of design methodologies for *self-correctable* and *self-testable* integrated RF/Mixed-Signal passive and active circuits embedded in System-on-Package (SOP), System-in-Package (SIP) and System-on-Chip (SOC) systems
- Designing RF receiver board/module with embedded active (ICs) and passives. In addition to the RF design understanding, this board design also requires understanding of signal integrity
- Designed self-correctable and self-testable LNA (SiGe) and Operational amplifier (CMOS)
- Research involves designing and modeling of RF active and passive circuits (RF amplifier, RF oscillator, RF filters) as well as understanding of packaging technology (SOP, SIP, SOC). Research also involves test-board design and validation of the newly developed test methods through measurements using vector network analyzer (VNA), spectrum analyzer and oscilloscope
- Developed low-cost testing methodology for RF passive and active circuits embedded in System-on-Package (SOP), System-in-Package (SIP) or System-on-Chip (SOC) systems
- Designed SMD/embedded RF filters (low-pass, high-pass and band-pass) using ADS and Sonnet. These filters were measured either with SMA or RF probes using vector network analyzer (VNA)
- Automated non-linear macromodeling based on neutral network for digital driver, digital receiver and differential drivers. Effect of simultaneous switching noise (SSN) was also included
- Modeled and Designed board-level feedback shift register circuits and parity checker. The testing was performed using Automatic Testing Equipment

### Relevant Courses

- Integrated Low-Cost Microelectronics Systems Packaging
- Microwave Design and Laboratory
- Digital MOS Integrated Circuits
- RF Engineering
- Advance Digital Testing
- Analog Integrated Circuits

## Selected Publications (total 12)

- Abhilash Goyal, Madhavan Swaminathan, Abhijit Chatterjee “A Novel Self-Healing Methodology for RF Amplifier Circuits Based on Oscillation Principles”, IEEE Design Automation & Test in Europe (DATE), April 2009
- Abhilash Goyal, Madhavan Swaminathan, Abhijit Chatterjee “Low-Frequency and Low-Cost Test Methodology for Integrated RF Substrates”, IEEE Transaction Advanced Packaging, pp. accepted (final revision)
- Abhilash Goyal, Madhavan Swaminathan, Abhijit Chatterjee, "Low-Cost Specification Based Testing of RF Amplifier Circuits using Oscillation Principles", Journal of Electronic Testing Theory and Applications (JETTA), pp. (accepted)
- Abhilash Goyal, Madhavan Swaminathan, Abhijit Chatterjee, “Low-Frequency Test Method for Integrated RF Substrates”, IEEE Electronic Components and Technology Conference (ECTC), May 2009
- Abhilash Goyal, Madhavan Swaminathan, "A Low Cost Method for Testing Integrated RF Substrates," IEEE International Microwave Symposium (IMS), June 2008
- Abhilash Goyal, Madhavan Swaminathan, Chirs Ward, George White, Abhijit Chatterjee, "A Novel Method for Testing Integrated RF Substrates," IEEE Asia-Pacific Microwave Conference (APMC), December 2007.

## Selected Patents/Invention Disclosures (total 4)

- Abhilash Goyal, Madhavan Swaminathan, Abhijeet Chatterjee, "A Novel Self-Healing Methodology Based on Feedback and Oscillation Principle," provisional application filed for GTRC ID 4773, in the USPTO.
- Abhilash Goyal, Madhavan Swaminathan, “A Low Frequency Low Cost Testing Methodology for Multi-Gigahertz RF Embedded Passive Filters via Inclusion into RF Oscillator Circuits,” provisional application filed for GTRC ID 4427, in the USPTO
- Abhilash Goyal, Madhavan Swaminathan, Abhijeet Chatterjee, "Low-Cost Testing Methodology for Multi-Gigahertz RF Embedded Passive Filters via Insertion into Feedback Network of Amplifier Circuits,” provisional application filed for GTRC ID 4327, in the USPTO

## Work Experience

2004 – 2005

### **Intel R&D Centre, India**

*Component Design Engineer*

- Lead the model release methodology for multi processor system. Focus of the methodology development was to release model every week automatically
- Performed functional validation of Advance Priority Interrupt Controller (APIC) at multi-core processor system (debug, checkers development, environment maintenance, test plan, e-test writing, and function coverage models development)

2002 – 2004

### **Texas Instruments, India**

*IC Design Engineer*

- Responsible for system and architecture level functional verification of SDIO interface bus (secure digital I/O 9 pin interface supporting SPI, SD1 and SD4 mode)
- Lead methodology development for functional verification of digital circuits. Focus of the methodology was to reuse prior developed verification environments to test new functional modules

## Computer Skills

### *Languages*

H-spice, Matlab, C, Verilog, E (Specman)

### *Tools*

- Advanced design system (ADS) and Sonnet for RF design
- Cadence tools for analog design
- Specman tool for digital functional validation
- Express PCB for multi-layer package layout

## References Available on request.