

## Kick-off Meeting:

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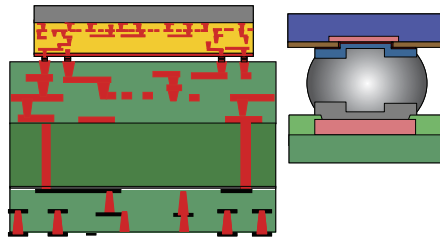
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## An Industry-Academia Consortium

# NGDP

## Next Generation Device Packaging



## MICROSYSTEMS PACKAGING RESEARCH CENTER

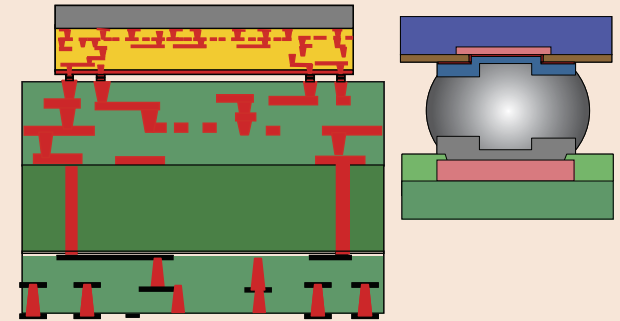
## Focus:

To investigate a total Interconnection, Substrate and Assembly solution for flip chip packaging of next-generation ultra low k-Cu and other devices that proposes to go beyond traditional flip chip interconnections by providing a total system-level solution based on novel concepts in electrical modeling, design and characterization, low stress interconnection and assembly materials and processes, advanced multilayer, fine pitch organic substrates with low-to-medium TCE, and thermo-mechanical modeling and design for reliability.

Sponsored by GT-PRC and IMEC, in collaboration with global industry, this consortium will seek to identify the key technology needs and solutions for next-generation flip chip scaling and packaging of the emerging Cu-low k and other devices.

## Proposed Topics:

- Interconnect Design
- Electromigration, Joule Effect
- Thermo-mechanical design and predictive



- modeling for zero stress
- Interconnection and Assembly Materials and Processes
- Barriers and interfaces for electromigration and stress control
- Novel underfill materials and processes for 20 micron flip chip and Cu-low k/ultra-low k
- Cu-ultra low k device assembly with flip chip and low-stress copper-based interconnections
- Multilayer Organic Substrate Process Technologies
- Next-generation interposers - substrates for interconnect / wiring and stress-relieved interconnections
- Thermo-mechanical Reliability
- Thermo-mechanical characterization on test vehicles
- Reliability testing and failure analysis

## Challenges and Uniqueness:

- Medium CTE organic and flexible substrates Integrated test vehicles for research demonstrations
- UBMs, barriers and Interconnect materials for reduced electromigration
- Novel low stress, high thermal conductivity and narrow gap underfill materials
- Thermo mechanical reliability at very fine pitch
- Chip-package co-design for electro migration resistance
- Integrated test vehicles for research demonstrations



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