The Perfection of System-on-Package (SOP) Printed Wire Board Fabrication

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Introduction

Today, there is an increasing demand for smaller electronic systems that accomplish even more functions then their larger predecessors. Under current technology the size of the superconductor chip cannot be made any smaller – the size is limited by the package, or the part that connects and links all the components together. The Georgia Tech Microsystems Packing Research Center is creating solutions to decrease the overall size of the system package by utilizing key processes like multilayer boards and imbedded resistors to decreases the total real estate of the system.

The Process

The process starts with the creation of the core and first copper layer. The boards are forged in a hot press. Five thin Teflon boards and copper foil are assembled and placed in the tool. The setting for the hot press has already been optimized for best performance. The entire hot press process takes about three hours with one increase in temperature and pressure in the middle. The copper foil that is laminated on is 18 microns (18 X $10^{\wedge -6}$ m) thick, which is thicker then required. The boards are etched down with the microetch to about range of nine or ten microns.

After the boards have been etched to the required thickness, the copper needs to be formulated into a pattern. A technique called Photolithography is used to form the patterns. Photoresist, a UV-light sensitive substance, is coated onto the surface. There are two different types of photoresist, dry film, and liquid. Both are sensitive to UV light and must be handled only in the yellow lights of the clean room. The dry film, or FX920, is laminated, while the liquid version, or NT-90, is spin coated on.

To expose the pattern a mercury-lamp powered exposure tool shines bright UV light onto the substrate. A Kevlar or glass plate, referred to as a mask, is placed over the board – just like a negative in traditional photography. The photoresist used is a negative type photoresist. Negative photoresist hardens when stuck by UV light hit and cannot be removed by the developer. But where no light hits the substance (the parts underneath the black areas of the mask) the photoresist will be able to be developed. FX920 the developer is 1% Na_2CO_3. For NT-90 a special company-made 'eagle' developer is used. The unwanted photoresist is stripped, and the pattern remains. Photoresist is a chemical seal which blocks the etch from removing the copper.

The boards are then etched removing all the copper expect for the copper that is underneath the photoresist. Then the remainder of the photoresist must be removed. A more powerful developer, the stripper, removes all the photoresist. Dry film is stripped with a 3% Sodium Hydroxide solution. After the etching and removal of all the photoresist, the board is prepared for the next layer. To separate the layers Benzocyclobutene (BCB) is spin coated on. The BCB is baked, and often put in the plasma tool.

For the first layer subtractive build-up is used -- the copper patterns are formed by etching. For the next layer subtractive etch cannot be used because there is no copper. The pattern must be additively built up. There are two processes to deposit copper on the boards – electroless and electrolytic. The electrolytic can plate more copper than electroless. However the electrolytic process requires a current to flow through the board and the polymer separating the two layers is a dielectric, or a non-conductor. To get around that problem initially a seed layer is placed before the photoresist is patterned.

This seed layer is formed using the Atotech Electroless Copper Line.

The Electroless Process:

1. Sweller – 5 min – Prevents the copper layers from peeling, and prepares the board for the Permanganate etch
2. Rinse – 2 min – Between most steps there is a cleaning step
3. Permanganate etch – 5 min – Removes particles on surface and roughens it up
4. Rinse – 2 min
5. Neutralizer – 2 min – Neutralizes the remains of the powerful permanganate etch
6. Rinse – 2 min
7. Condition – 5 min – Prepares and cleans the board
8. Rinse – 2 min
9. Rinse – 2 min
10. microetch – times vary (15-30 sec normally) – removes small amount of copper (about .5 micron)
11. Rinse – 2 min
12. Predip – 1 min
13. Activator – 4 min
14. Rinse – 2 min
15. Reducer – 4 min – Boric acid and a company made 'neograph reducer'
16. Rinse – 2 min
17. Electroless Cu – Times vary – The plating bath: $CuSO_4$, NaOH, Formaldehyde, and others to stabilize the bath.
18. Rinse – 2 min
19. Acid Dip – 1 min – 10% Sulfuric acid
20. Rinse – 2 min
21. Antitarnish – 1 min – to prevent future oxidation.
22. Final rinse

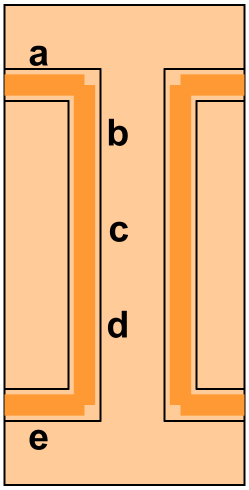
The electroless-line requires constant maintenance. The concentration of each chemical in every bath must be kept at certain levels. The electroless copper (process number 17) bath's concentration levels must be checked every time before it's used, and proper additions must be made to ensure it will work optimally. To verify if the bath is operational three titrations are done. The first titration checks for the copper level concentration. The ideal level is 50 g/L, but there is an operating range. If the concentration level is too low, Copper Soln PT part A is added. The second titration tests the PH. The PH should be 13.6. To compensate for decreased PH, sodium hydroxide is added. The final titration checks for the concentration of the reduction solution in the bath. The desired concentration of the reduction solution is 16 ml/l. The reduction solution is primarily composed of formaldehyde, a key component to the plating bath. It reduces the Cu^{2+} to Cu metal on the surface of the board. It must be added slowly, or the bath will crash.

Copper Pulse Bath

During my stay at PRC a new type of electrolytic bath was set up. The old type has some drawbacks. The copper plates more at the corners near the anode and cathode, and less in the center. It creates an uneven layer. Copper Pulse, the new type, first sends a pulse of the current in the forward direction then in the reverse direction, which removes some of the copper that was plated. Thus by going back and forth, like a tug of war game, it plates the board evenly. In the copper pulse bath the copper content is about 22 g/l, and it has a high sulfuric acid content, as opposed to the electroless bath, which has a higher copper content, but no sulfuric acid.

After the new Copper Pulse bath was up and running, test boards were dummy plated as an initial testing produced to examine the effectiveness of the plating in the through holes. There are multiple parameters that can be changed; including the forward and reverse time, and the power for each. For the qualification tests we ran the dummy boards at 15 Amps per square foot.

Measurement Locations:

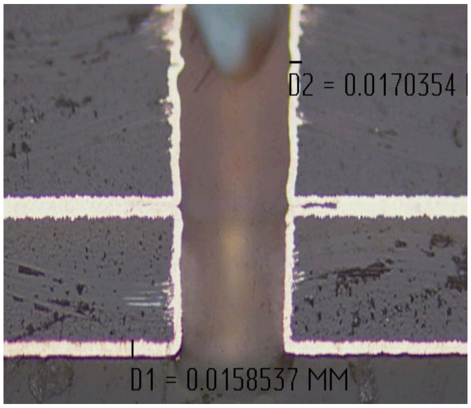


Amp Hours	Copper Thickness (microns)	Process Conditions
300	(a) 13.7 (b) 15.8 (c) 17 (d) 11.1 (e) 13	FWD 10 Amps,10.0ms REV 10 Amps, 0.5ms 15A/ft^2 1 hour total plating time
1000	(a) 20.7 (b) 21.9 (c) 15.5 (c) 17 (d) 20 (e) 18.5	

Research Assistant

As a research intern it was my job to assist in the board fabrication process. I learned to operate the hot press, spin coater, exposure tool, electro-less line, plasma tool, lamination machine, technic line, and the photographic microscope. In addition, I further developed my chemistry skills by creating and preparing solutions like the photoresist stripper, and doing regular titrations. Besides helping in the actual plating process, I aided the general-lab-maintenance team to set up labs, titrate and correct baths and clean up waste. After a board was finished a cross section often was needed to measure the microvia thickness. A cross section is a board, cut and dried into a polymer sample. Pictures and measurements can then be taken with a microscope.

A cross section of the 300 Amp Hour Dummy Board:



Conclusion and Acknowledgements

The process of fabricating multilayer boards with blind and micro via technology is improving, but is far from perfect. My work and assistance will join the work of others to help achieve PRC's goal of enhanced next generation systems package.

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