Fabrication of Decoupling Capacitors using Polymer/Ceramic Nano Composite Process for Microelectronics

James Wang
Advisor: Dr. Robin Abothu
Staff: Dr. Swapan Bhattacharya and Mr. Venky Sundaram
Grad Student: Dev Balaraman

Introduction

A passive device is defined as a device that does not require an energy source for operation. They can be resistive, capacitive, or inductive; others may include diodes, optical fibers, cables, wires, filters, and glass lenses. Integral passive offers numerous advantages such as increased silicon efficiency, improved electrical performance, elimination of separate packaging (no assembly to board soldering and thus increased reliability), and efficient circuit design. However, these benefits demand extremely high product yield at reduced cost. The focus of this project is confined to fabrication, and electrical performance of capacitors on organic substrates.

Capacitors integrated on low-loss organic package substrates can find numerous RF and microwave SOP applications (such as VCO, IF/RF bandpass filters, LNA, etc), in which IC chips are flip-chip mounted on the package substrate. To address the high capacitance density requirements of integral capacitors, a series of organic and inorganic based materials that are compatible to organic based laminate process has been developed [1]. A capacitance density of ~30 nF/cm^2 has been achieved in polymer/ceramic nanocomposites through optimization of particle dispersion. For higher capacitance densities (>200 nF/cm^2), hydrothermal synthesis of barium titanate particles and deposition of non-stoichiometric inorganics by metal-organic chemical vapor deposition showed promising results.

Significant size reduction and improvement in electrical performance of microelectronic systems can be realized through integration of passive elements like capacitors, resistors and inductors. Integration of capacitors poses unique challenges because of the need for a wide range of capacitances (from 0.1 pF to 10 μF) and low dielectric losses. Nearly 50 % of these capacitors will be used as decoupling capacitors which requires 0.1 – 10 μF and are the hardest to integrate on organic boards. A number of existing material systems, like polymers with low dielectric constant and loss stable with frequency, can be used for embedding small capacitance values. Further, these polymers can be filled with ferroelectric powder, resulting in a polymer-matrix composite with processable capacitance density up to 5-10 nF/cm^2. The focus of this work is to develop and implement nano-composite process for System-On-Package application.

Nanocomposite Approach

The PRC began to pioneer the polymer-ceramic nanocomposites technology as a highly favorable low-cost option for embedded capacitors in organic laminates because of its low processing temperature (<200°C) and cost advantages. Nanocomposite dielectrics are essentially dispersions of nano-sized particles (< 200nm) in a polymeric phase. The cornerstone of this technology is the development of defect-free thin films (<2 microns) with a high packing density of the ceramic filler. High ceramic filler content (>50 vol%) is needed in order to achieve a high dielectric constant.

Experimental:

The flow chart for the fabrication of nanocomposite capacitors has been depicted in Figure 2. The slurry for the spin coating of capacitor film has been prepared by mixing 44 gms of polymeric resin which contains barium titanate (Product No: XB 7191) with 4.24 gms of hardener (Product No: XB 7228) along with 5 gms of thinner (Probele 81/7081) all from Ventico company. The mixture was then allowed to settle in order to get rid of bubbles and then spin coated using spin coater (Fig 2 (a)) on 6x6" copper plated boards at 1900 rpm, 2100 rpm, 2500 rpm for 30 seconds. The thickness of the film has been measured by DAKTEC profilometer (Fig 2 (b)) The spin coated boards were then baked at 65°C for 45 mins and laminated with copper foils using vacuum laminator (Fig 2 (c)) followed by hot press using 2 tons of pressure at 158°F for 20 minutes. The boards were then treated for bond film and laminated with FX515 dry film with vacuum laminator. The boards were exposed with mask under UV exposure tool (Fig 2 (d)) for 15 seconds and developed at 45C. The copper was then etched through the photo resist opening. The board was then rinsed and dried followed by stripping FX515 with 3% NaOH at 55C. The boards were then rinsed with water and dried and flood exposed under UV tool for 2 minutes. Finally the boards were developed with GBL spray bottle followed by rinsing with isopropanol and water and cured at 150C for 60 minutes. The capacitance values of the fabricated capacitors were measured using LCR meter at lower frequencies.

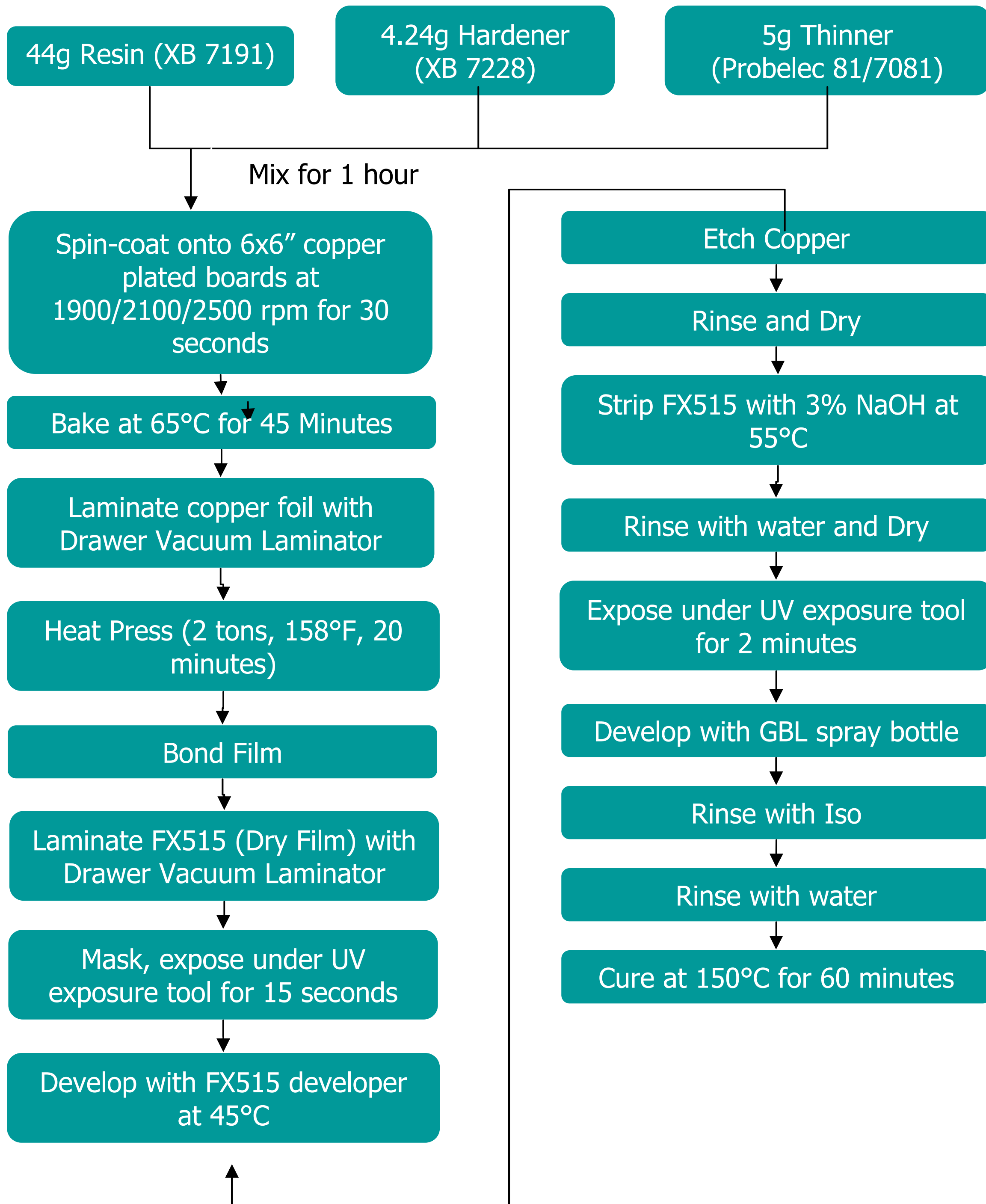


Figure 2. Flow chart for the fabrication of nanocomposite capacitors

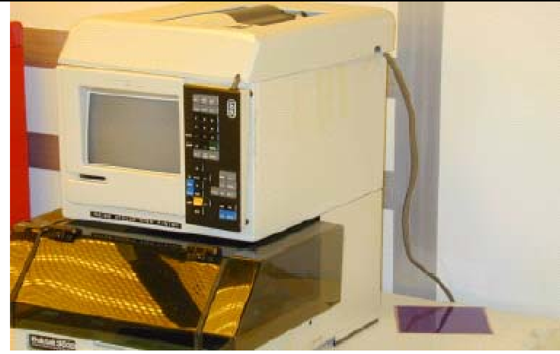
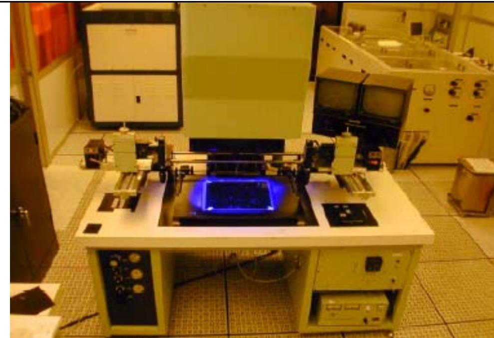
<table>
<tr><td>
(A) Spin Coater</td><td>
(B) DAKTEK Profilometer</td></tr>
<tr><td>
(C)Drawer Vacuum Laminator</td><td>
(D)UV Exposure Tool</td></tr>
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Figure 2. Clean room equipment used in this project

Results and discussion:

Figure 3 shows the fabricated capacitors on organic board. The dielectric data of the nanocomposite capacitor has been tabulated in Table 1. From the table it is clear that capacitance values increases with decreasing film thickness as can be expected from equation:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}$$

Area of the plate

Capacitance

Permittivity of free space

Relative permittivity

Dielectric thickness

The loss factor does not change much since the material property remained constant. The adhesion of the dielectric to the copper bottom electrode and on the top electrode as good as evident by the scotch tape test. The photo definition of the capacitor material was better since no ceramic particles were observed after the GBL treatment. The copper was very clean. The fabricated capacitors are depicted in Figure 3.

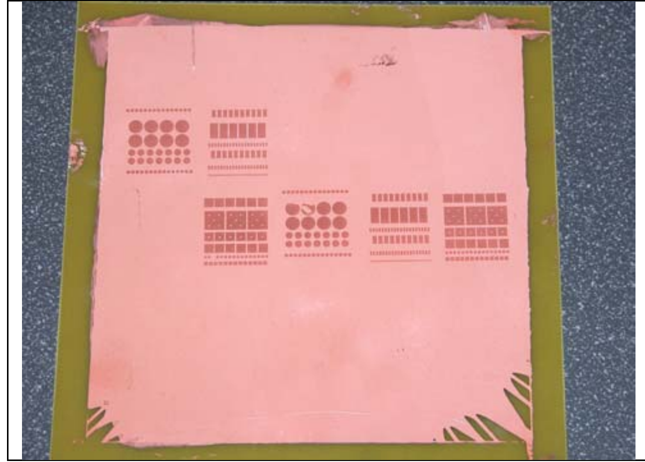

Figure 3: Nanocomposite capacitors on organic board

Table 1. Dielectric data of fabricated thin film capacitors

First Board (20 microns)							
Largest Circles			Second Largest Circle			Largest Square	
Capacitance (pf)	Loss		Capacitance (pf)	Loss		Capacitance (pf)	Loss
109	0.017		26.44	0.02		247	0.019
97	0.017		25.28	0.02		256	0.019
Second Board (8 microns)							
Largest Circles			Second Largest Circle			Largest Square	
Capacitance (pf)	Loss		Capacitance (pf)	Loss		Capacitance (pf)	Loss
238	0.016		57.8	0.01		545	0.017
241	0.017		55.7	0.01		573	0.016
			55.5	0.01			

Conclusion:

We have Optimized process conditions for thinner films to obtain higher capacitance of 1.5 nF/sq cm. This process is inexpensive for top metal electrode using metal foil lamination and combined process for large area fabrication of System-On-Package (SOP) boards.

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2. H. Windlass, P. Raj, D. Balaraman, S. Bhattacharya, R. Tummala, "Processing of Polymer-Ceramic Nanocomposites for System-On-Package Applications", 51st ECTC, Orlando, Florida, May, 2001, pp 1201-1206.