

# Impact of 3D ICs with TSV is profound but complex and costly - is there a better way?

By Rao R. Tummala and Venky Sundaram

At Georgia Tech PRC, we think so; we call it 3D interposer. Unlike 2.5 interposer, the 3D interposer does not require through silicon vias (TSVs) in the logic chip. It is based on ultra-thin interposers that are the same thickness as the individual chips in the 3D IC stack; about 30µm. It has through vias that are the same diameter and same pitch as TSVs in the 3D ICs — about 5-10µm diameter on 15-30µm pitch. Unlike 3D ICs with TSV, however, the Georgia Tech (GT) approach is scalable, testable, and presents less thermal problems than the 3D IC stacks. It is also cheaper.

3D ICs with TSV are being widely developed around the world for two reasons. First of all, heterogeneous integration of logic, memory, graphics, power and sensor ICs requires it since these functionalities cannot be integrated into a single chip. Secondly, 3D ICs with TSVs offer improved electrical performance due to the short interconnect and ultra-high number of TSV interconnections between stacked ICs to address the perceived engineering limits in leakage and electrical performance of CMOS ICs beyond 11-16nm. But these benefits come at very high cost and with significant disruption in wafer fabs. Additionally, the 3D stack presents major technical and manufacturing challenges that include testability and yield, scalability, along with thermal and standardized IC interface challenges. The electrical performance improvement with 3D ICs is temporary. Intel has already announced that it will develop FinFET to overcome the shortcomings of traditional CMOS, to continue Moore's Law beyond 11-16nm. Improved performance alone is no longer a good argument for 3D ICs or heterogeneous ICs.

Georgia Tech PRC proposes and demonstrates an entirely different concept;

one that addresses many of the above challenges and allows packaging of ICs without disruption to wafer fabs. **Figure 1a** illustrates the current approach to 3D IC stacking with TSVs on an interposer such as silicon. In contrast, **Figure 1b** shows GT PRC's approach, which is based on an ultra-thin, double-side 3D interposer, made of either low-cost ultra-thin polycrystalline silicon or low-cost ultra-thin glass, not in 200-300mm wafer form but in large, 450-700mm panel form. Since the interposer is identical to one of the 3D ICs in the 3D stack with regards to through-via interconnection length and interconnect density, it behaves like a 3D IC stack with TSV. Such an approach does not require TSV in the logic chip yet it achieves the same bandwidth as 3D ICs with TSVs by virtue of logic on one side and memory stack on the other side interconnected and separated by the 30µm thick interposer. **Figure 2** shows the superiority of GT approach over the 3D ICs with TSV in

signal delay between logic and memory as well as over wafer-based silicon interposers with thin oxide liner. In addition, the 3D interposer approach allows for testability first of the interposer itself, followed by testing with memory stack and then with logic chip or vice versa. The 3D interposer approach is scalable by simply attaching chips side by side on both sides interconnected by ultra high I/O redistribution layers (RDL) made of 0.5 to 5µm wiring. The thermal management problems are simplified as well by virtue of separating the logic IC from the memory stack. The single most important benefit of this approach is a cost reduction by a factor of 5-10X over silicon interposers fabricated out of wafer fabs, as illustrated in **Figure 3**. Contributing reasons are many and include large panel, low cost through-via processes, and low cost RDLs.

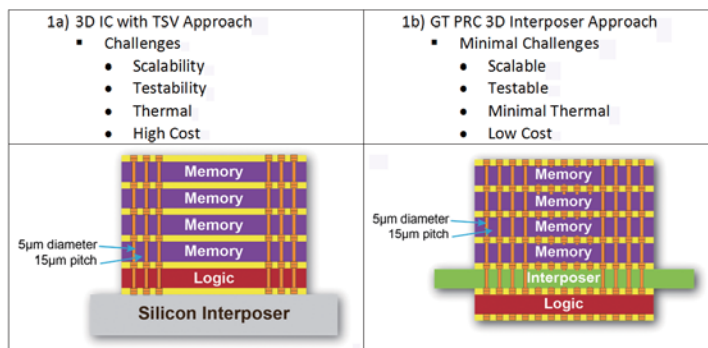


Figure 1a. 3D IC with TSV approach  
Figure 1b. GT PRC 3D interposer approach for bandwidth<sup>1</sup>

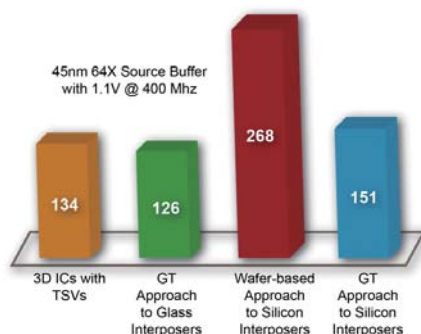


Figure 2. Superiority of GT 3D interposer approach over traditional silicon interposers and 3D ICs in signal delay (PS) between logic and memory

## 3D Glass Interposer Technology

Glass has many advantages as an interposer material over silicon; namely ultra-high resistivity and availability in thin and large sizes. It is used as a thin and large panel in LCD displays, and thin-film metallization onto glass panels is well known in plasma displays. It has excellent resistivity on par with SiO<sub>2</sub> and is available in a variety of compositions with TCE ranging from

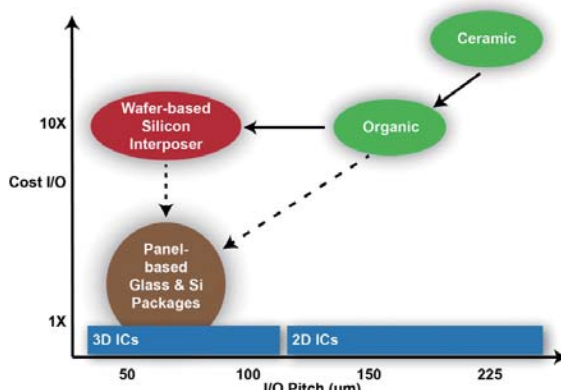


Figure 3. GT PRC panel-based strategy for low cost of 3D silicon and glass Interposer vs. wafer-based silicon interposer (courtesy of Tummala)

3ppm, matching silicon IC, to 9ppm, in between silicon IC and organic board. The main technical barriers of glass interposers are how to form large and ultra-thin glass panels, through-package-via (TPV) holes at high throughput, and how to handle ultra-thin glass panel substrates. For some applications, low thermal conductivity, although higher than current organic polymer interposers, may be another barrier.

Recently, numerous glass companies have developed new and innovative processes for forming large and thin glasses in a variety of compositions. Laser ablation and photosensitive glasses for the formation of via holes are two of the most promising processes. Laser ablation provides small vias in glass but has conventionally been a serial process. GT PRC, in collaboration with one of its industry partners, demonstrated, for the first time, a parallel via formation method. This method enabled formation of more than a thousand vias simultaneously within few seconds. The result was a 33x33 (1089) through-via array of 19µm on 30µm pitch, drilled simultaneously in 55µm thin borosilicate glass.<sup>2</sup>

### 3D Silicon Interposer Technology

Table 1 compares and contrasts the GT PRC approach to the traditional wafer-based industry approach for silicon interposers. In general, the GT PRC approach to 3D silicon interposers has the potential to achieve equivalent interconnect density at significantly lower cost by a factor of 5-10X, by using the following:

- 1) Large panel-based substrate up to 450-700mm in size

- 2) Cheaper polycrystalline silicon
- 3) Low-cost TPV process without DRIE
- 4) Low-cost thick polymer liner
- 5) Low-cost, double-side RDL process.

The high I/O routing capacity combined with the low cost of GT PRC's approach to glass and silicon interposers presents a number of application opportunities, both in mobile and high performance systems. Applications include mixed function digital logic-memory, RF, analog and MEMS in mobile applications. Additionally,

glass and silicon interposers can be applied for high performance applications requiring more than 10,000 I/Os between multiple logic ICs placed side by side in the same large package, as big as 50-70mm in size.

### Industry Consortium at Georgia Tech PRC

3D interposer R&D is being performed at GT PRC under an industry consortium that includes the following companies to date: Asahi Glass, Atotech, Corning Glass, Dupont, EVG, Henkel, Life BioScience, Maxim, Namics, Qualcomm, Rogers, Schott Glass, Shinko, STMicro, and Zeon Corp. These companies fall into a complete supply chain for glass or silicon material, via hole formation tools, via metallization processes, RDL materials and processes, metalized substrates, package integrators or end users.

### Summary

The 3D interposer presented here makes a compelling case for the 3D interposer over both 3D IC stacks with TSV as well as over traditional wafer-based silicon interposers.

It doesn't require a new business model of having multiple ICs from different vendors to be integrated into one standardized 3D IC stack. It is scalable, testable and offers thermal solutions in a traditional way. There is no disruption to wafer fabs or loss of real estate within the CMOS chip to accommodate TSVs. While the initial concepts have been demonstrated at Georgia Tech, it requires additional R&D, and additional industry partnerships with both manufacturing and end user companies.

### References

- [1] G. Kumar, et al., "Ultra-High I/O Density Glass/Silicon Interposers for High Bandwidth Smart Mobile Applications," Proceedings of 61st Electronic Components and Technology Conference, 2011 May 31-June 3, Lake Buena Vista, FL 217-223.
- [2] V. Sukumaran, et al., "Design, Fabrication and Characterization of Low-Cost Glass Interposers with Fine-Pitch Through-Package-Vias," Proceedings of 61st Electronic Components and Technology Conference, 2011 May 31-June 3, Lake Buena Vista, FL 583-588.
- [3] Q. Chen, et al., "Design and Demonstration of Low Cost, Panel-Based Polycrystalline Silicon Interposer with Through-Package-Vias (TPVs)," Proceedings of 61st Electronic Components and Technology Conference, 2011 May 31-June 3, Lake Buena Vista, FL 855-860.

	Industry Approach	GT Approach
Substrate	Single crystalline silicon wafer	Polycrystalline silicon panel
Size	300mm	450~700mm
Thickness	50µm with chem-mech polish	50-200µm without chem-mech polish
Hole Formation	DRIE	Laser
Liner Formation	SiO <sub>2</sub> by CVD + Barrier layer by PVD	Polymer filling and laser via
Seed Layer	PVD	Electroless plating
RDL	BEOL	Dry film and plating

Table 1. Wafer approach to silicon interposer vs GT approach to silicon interposer for lower cost and higher Performance.<sup>3</sup>