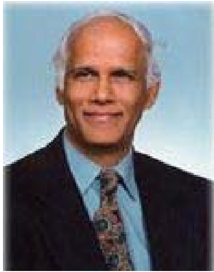

# Georgia Tech's Vision for Ultra-miniaturized Device and Systems Packaging

## Encompassing R&D, Inter-disciplinary Education and Global Collaborations

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Moore's Law began with transistor integration at IC level in the late 1940s. Georgia Tech's 3D Systems Packaging Research Center (GT PRC) has launched a new era of Moore's Law for system integration with the System-On-Package (SOP) concept.

There are two primary reasons for SOP. First, is functionality and miniaturization at package and system levels. There has been phenomenal progress made at the IC level from 2500nm technology in the 1970s to 32nm and beyond, resulting in a billion transistor IC. However, the packages and system boards that house these and other devices and components are almost a billion times bigger in lithographic ground rules than the ICs themselves.

The second reason for SOP is lack of quantum jump in electrical performance or functionality at the system level. The SOP vision eliminates the IC-system gap (**Figure 1**) using nanoscale materials, processes, and unique properties that are produced for every component of the system. This includes interconnections; thermal interfaces; passive components such as capacitors, resistors, filters, and batteries. The SOP concept is expected to revolutionize system functionality in smallest size and at lowest cost, thus complementing system-on-chip (SOC) at the IC level and 3D integrated circuits (3D ICs) at module level (**Figure 2**). **Figure 3** is PRC's vision of SOP-based system with all its nanoscale system technologies.

In contrast to traditional academic research by faculty and graduate students alone, Georgia Tech PRC has pioneered an integrated approach with cross-discipline education of students at BS, MS and Ph.D levels and industry collaborations with more than 70 companies from the US, Europe and Asia — all in SOP.

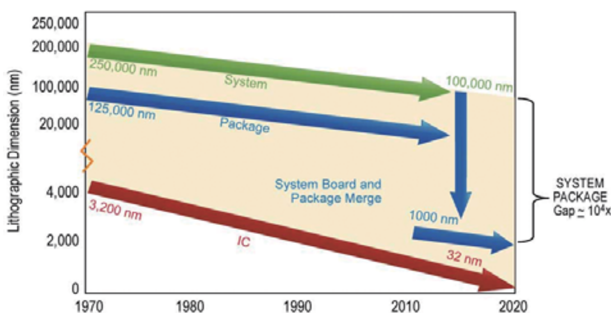


**Figure 1.** SOP merges package and board close to IC ground rules

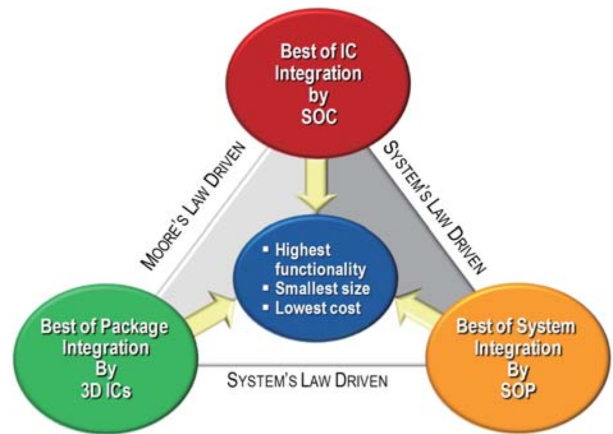


**Figure 2.** SOC for ICs, 3DICs for modules and SOP for systems

## Seven core packaging technologies

To explore and demonstrate a futuristic system, PRC focuses on seven core research areas including electrical design, mechanical design, nano-scale materials and processes, nano-scale components, advanced substrates, interconnections, and system integration.

## Electrical design

The electrical design team vision and strategy is to model and design ultra-miniaturized modules and systems using SOP technologies (**Figure 4**). The research focus includes electromagnetic modeling; signal and power integrity modeling and analysis, and design of embedded actives and nanoscale digital and RF passive components; ultra miniaturized pad-to-pad interconnections; low-loss dielectrics; and high-speed signal channels in electronic, optical, and MEMS packages. The electrical design is aimed at a wide range of packaging technologies such as organic, glass and silicon packaging.

Currently, two focus areas include electrical design of ultra-miniaturized and high-density organic packages with chip-last Embedded MEMS, Actives, and Passives (EMAP). The actives include multiple embedded digital, analog, RF,

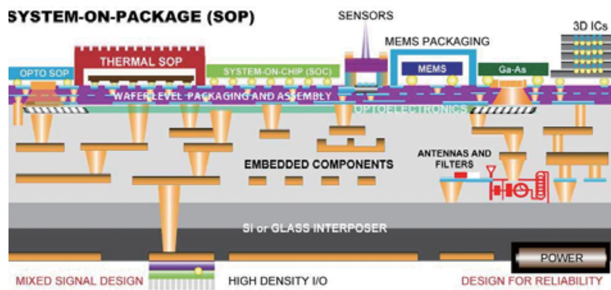


**Figure 3.** PRC's vision of SOP with the necessary core technologies

**Figure 4.** Electrical design focus

and MEMS. The electrical design team has demonstrated high Q (Q>100) inductors (1-10GHz) in 100µm thick (2-metal layer) and 160µm thick (4-metal layer) low-loss organic substrates; as well as band pass filters (2.4 and 5.8 GHz bands) with insertion loss <1dB and rejection 25dB. In development are solutions for power integrity, electromagnetic interference and noise coupling problems in packages with embedded active chips.

The electrical design of low-cost silicon and glass packages to package 3D ICs is supported by a global industry consortium of approximately 10 companies. The focus here is in the development of high-performance and ultra-miniaturized packages with highest through-package-vias (TPVs) and highest I/O density. Accurate electrical models for TPVs in silicon substrates have been developed. Novel electrical designs for power, signal, and clock distribution are being developed utilizing the semiconductor effects.

## Mechanical design

Up-front mechanical design from first principles coupled with experimental reliability assessment is the PRC's strategy for mechanical design in a systematic flow, beginning with process modeling (**Figure 5**).

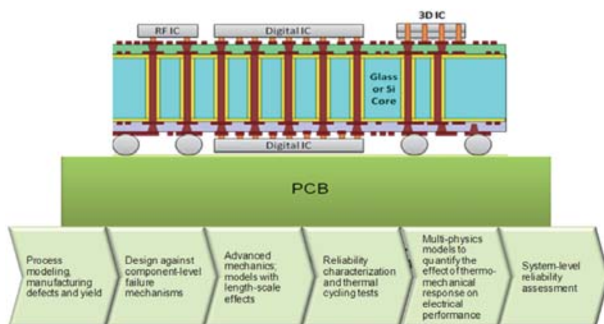


**Figure 5.** PRC's systematic process for mechanical design

For example, in the development of silicon and glass packages with TPV technology, upfront physics-based process mechanics and design-for-reliability models for various failure mechanisms are developed to evaluate various design, material, and process options even before the prototypes are made. Materials display strong scale effects when the characteristic length scale associated with non-uniform plastic deformation is on the order of microns. For example, in the mechanical design of copper TPVs with the diameter in the order of 10-25µm, the traditional continuum-based modeling techniques need to be augmented with models that incorporate the copper micro-scale hardening effects.

## Nano packaging materials

Traditional packaging materials such as for dielectrics and thermal interfaces; and passive components such as capacitors, filters, and antennas, have fundamental limitations in achieving the best property in smallest size. Over the past five years, PRC has explored a number of nanomaterials to address these two barriers (**Table 1**).

| Components | Today's materials | Nanomaterials research at GT PRC |
|---|---|---|
| Capacitors | Sputtered and solgel thin films<br>1-2 µF/cm$^2$ | • Nanoscale electrodes<br>• Conformal nanodielectrics<br>• 100 µF/cm$^2$ |
| Inductors | Sputtered and plated metals<br>100 nH/mm$^2$, 10 MHz | • Magnetic nanocomposites and nanowire arrays<br>• 1000 nH/mm$^2$, 100-1000 MHz |
| RF dielectrics | LTCC, LCP, PTFE, BCB<br>Permittivity: 2.5-8<br>Permeability: 1 | • Nanoscale super-paraelectric and super-paramagnetic materials<br>• Multiferroic materials<br>• Permittivity: 20-100<br>• Permeability: 5-100 |
| Interconnections | Solders<br>150µm-pitch reliability | • Nanometal and nanocomposite interconnections<br>• 20-50µm-pitch reliability<br>• 150-250°C processing |
| Batteries | $LiCoO_2$, LIPON, Li-C<br>0.1 mAhr/cm$^2$ µm | • Nanoelectrodes<br>• Super-ionic conductors<br>• 1 mAhr/cm$^2$ µm |
| Thermal Interfaces | Thermal grease, solders<br>0.1°C cm$^2$/W | • CNT based and nanocomposite TIM<br>• 0.001°C cm$^2$/W |

**Table 1.** Focus of Nanopackaging Materials Research at GT PRC

## Nano-scale components

Electronic systems require many components including actives, passives, thermal structures and batteries, as well as interconnections to interconnect all these and more to form systems. The current approach uses bulky milliscale components and are therefore the biggest bottlenecks for enhancing system functionality per unit area, performance as defined by speed or bandwidth, and power consumption as defined power losses. **Figure 3** illustrates some key component technologies in the SOP concept, and a brief description of PRC's nanocomponents focus in power supply components is provided here.

Thin-film capacitor for decoupling and voltage regulation has been one of the greatest barriers for system miniaturization and enhanced-digital performance. This is due to lack of low-cost, low-temperature, thin-film material

and process technologies with high permittivity at high frequencies compatible with silicon and organic substrate technologies. Over the past decade, GT-PRC has advanced high-density thin-film capacitors using low temperature, organic or IC-compatible processes. High-permittivity, thin-film dielectrics by themselves are not adequate to achieve higher capacitance densities with high reliability, so the industry is shifting to trench capacitors. To address the cost and throughput limitations of these approaches, PRC has pioneered novel nanostructured electrode and conformal dielectric technologies to achieve capacitance densities around 50-60 uF/cm$^2$ at high voltages. This exceeds what has been achieved with trench and tantalum capacitors in terms of volumetric efficiency. Power conversion for portable applications demanding high current supply with high efficiency largely depends on inductive energy storage elements. At this time, inductors on silicon do not meet the Quality Factor (Q), size, magnetization, and frequency requirements for many power electronic applications. Novel magnetic nanocomposite cores with innovative silicon and organic substrate-compatible 3D fabrication techniques for enhanced inductance densities and magnetization are being developed by PRC to miniaturize inductors while retaining their high frequency stability and high Qs.

## Package substrates

Substrate technology is the first building block with which to integrate all other system components. **Figure 6** illustrates the trend beginning with leadframes and plastic packages in the 1970s, high temperature co-fired ceramics (HTCC) in the 1980s, glass-ceramics or low temperature co-fired ceramics (LTCC) in the 1990s, and most recently build-up thin-film organic packages.

Organic packages, currently considered the most leading-edge, are reaching limits in I/Os because of poor dimensional stability, thus requiring large capture pads for layer-to-layer interconnections. These problems are easily addressed by silicon interposer technology developed worldwide using 200 and 300mm wafers. While silicon interposers solve the I/O density problem, it is not at a low enough cost per I/O to be a pervasive technology (**Figure 7**). The GT PRC proposes to solve both the I/O density and cost problems by panel-based, low-cost material and process approaches with both silicon and glass packages.

Glass as a package substrate material provides excellent dimensional stability, highest electrical resistivity (insulator), Si-matched CTE and is available in thin and large panel format. Non-CMOS grade panel-based silicon is also an excellent package substrate with high thermal conductivity and dimensional stability, as well as matched CTE to Si. A double-side, panel-based fabrication approach using low-cost materials is being developed with optimal electrical, mechanical, and thermal performances. The main challenge with both Si and glass is how to form through vias at low cost.

## Interconnections, assembly and reliability

The main drivers for innovation in high-reliability device and system interconnections are increased I/O density, high-

Figure 6. Evolution of packages for increased I/Os and lower cost

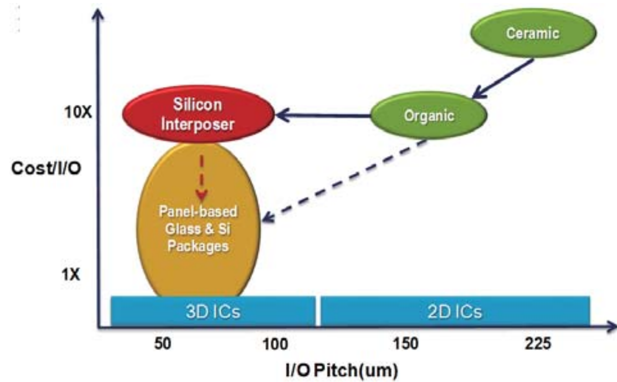


Figure 7. GT PRC's approach to low-cost Si and glass packages

throughput tools, and low-cost materials and processes. Therefore, interconnection research at PRC focuses on ultra-miniaturized, highly reliable, fine-pitch, low-profile and low cost materials and processes (**Figure 8**). This research falls into two major areas: chip-to-package and package-to-board.

The PRC strategy in chip-to-package interconnection is to design from first principles to achieve 10-40x higher I/O density than traditional flip-chip assembly in two ways:

1. *Chip-last copper-to-copper interconnections*: The goal of this research is to explore and demonstrate highly reliable ultra-fine pitch (~30µm) Cu-Cu interconnections bonded to organic substrates at low temperatures (160°C). The interconnect structure has been shown to pass reliability tests such as thermal cycling test (TCT), high temperature storage test (HTS) and un-biased highly accelerated stress test (U-HAST), as well as 2000 thermal cycles from -55°C to 125°C.

2. *Reactive nano-particle based pad-to-pad interconnections*: The objective of this project is to enable extremely fine (<10µm) pitch pad-to-pad interconnections at low-temperatures (<250°C) using ultrathin "bumpless" thin metal as the reactive bonding layer. The nano-metal layer enhances the reactivity, thus lowering the bonding temperature. This research addresses several of the fundamental limitations of today's flip-chip technology such as pitch, processing cost, thermo-mechanical reliability and electromigration resistance. It also overcomes the challenges of direct Cu-to-Cu bonding technology requiring high-temperature (400°C) bonding, plasma cleaning of surfaces and long annealing times.

In the package-to-board interconnections, PRC's strategy is to explore and demonstrate SMT-compatible interconnections for silicon-to-board or glass-to-board interconnections. This research is being performed with a variety of options that include low-modulus solders and zero-stress interconnections.

## System integration

The system integration research at PRC aims to integrate all these novel technologies into first proof-of-

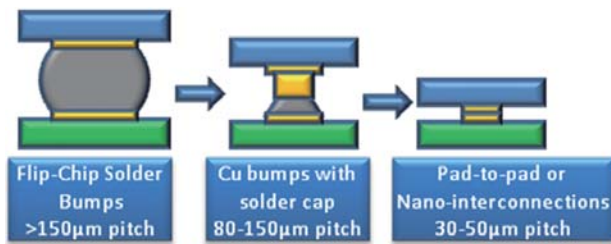

**Figure 8.** PRC strategy for interconnection research

concept packages or modules.

The PRC strategy in system integration begins with design from first principles leading to a set of research targets for materials, processes, and structures. Miniaturization challenges addressed include isolation of components at close proximity, high reliability interconnections at fine pitch, thermal dissipation of embedded active and passive components, and involvement of supply chain companies for materials and design tools to provide a path for manufacturing infrastructure.

Going well beyond fundamental research and individual leading-edge technologies, PRC has assembled an interdisciplinary team of academic and research faculty, industry engineers serving as mentors to BS, MS, and Ph.D students to demonstrate the first-of-its-kind digital-RF-optical integrated system to transmit and receive on a single module called Intelligent Network Communicator (INC). This demonstration of 3.1Gbps digital data rate, 5.8GHz RF front end, and 10Gbps optical data rate was achieved in a small form factor SOP package of 50mm x 75mm (**Figure 9**).

## Interdisciplinary education

The ultimate goal of PRC's educational vision is to produce "cross-discipline individuals."

Georgia Tech's comprehensive and inter-disciplinary educational programs in packaging include courses, curricula, textbooks, certificates and degrees. Each PRC student is educated with an interdisciplinary focus combining electrical, mechanical, chemical and materials sciences and engineering knowledge because electronic systems are interdisciplinary by nature.

## Global Industry Collaborations

The PRC's vision for industry collaboration includes not only R&D but also intellectual property development, manufacturing infrastructure development involving supply chain companies, facilities-usage, and human resource development at the BS, MS and Ph.D levels. In contrast to the industry's internal R&D that focuses on the three-to-five years prior to manufacturing, industry collaborations at PRC focus beyond five years because most new technologies take longer than five years of R&D before being ready for manufacturing. This process starts with exploration of new ideas by PRC's research team before coupling with industry for their strategic technologies in one of two ways: through establishment of research consortia for strategic technology developments; and infrastructure and network consortia for all others. Currently, there are two primary industry research consortia involving more than 25 global companies at the PRC: one in Embedded MEMS, Actives and Passives (EMAP) and the other in panel-based, low cost silicon and glass packages. A third and soon-to-be-launched program, called Industry Partnership in Packaging (IPP), seeks to involve more than 50 global-networked companies to develop infrastructure needed for future of packaging industry.

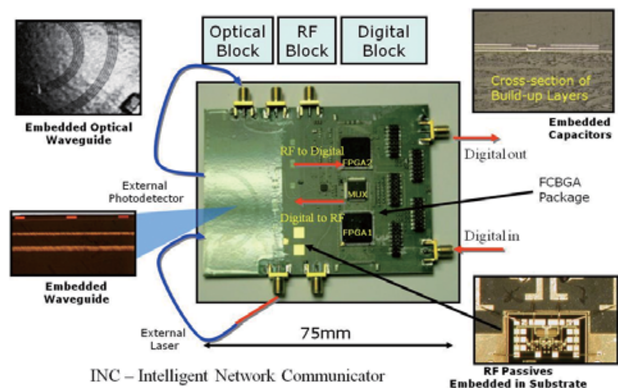

**Figure 9.** First Digital-RF-optical SOP demonstration at PRC

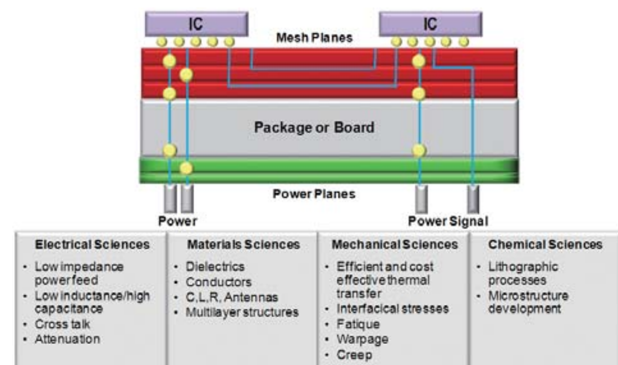

**Figure 10.** Cross-discipline education at GT PRC

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