



International Electronics Manufacturing Initiative

2005 SIP Roadmap Overview



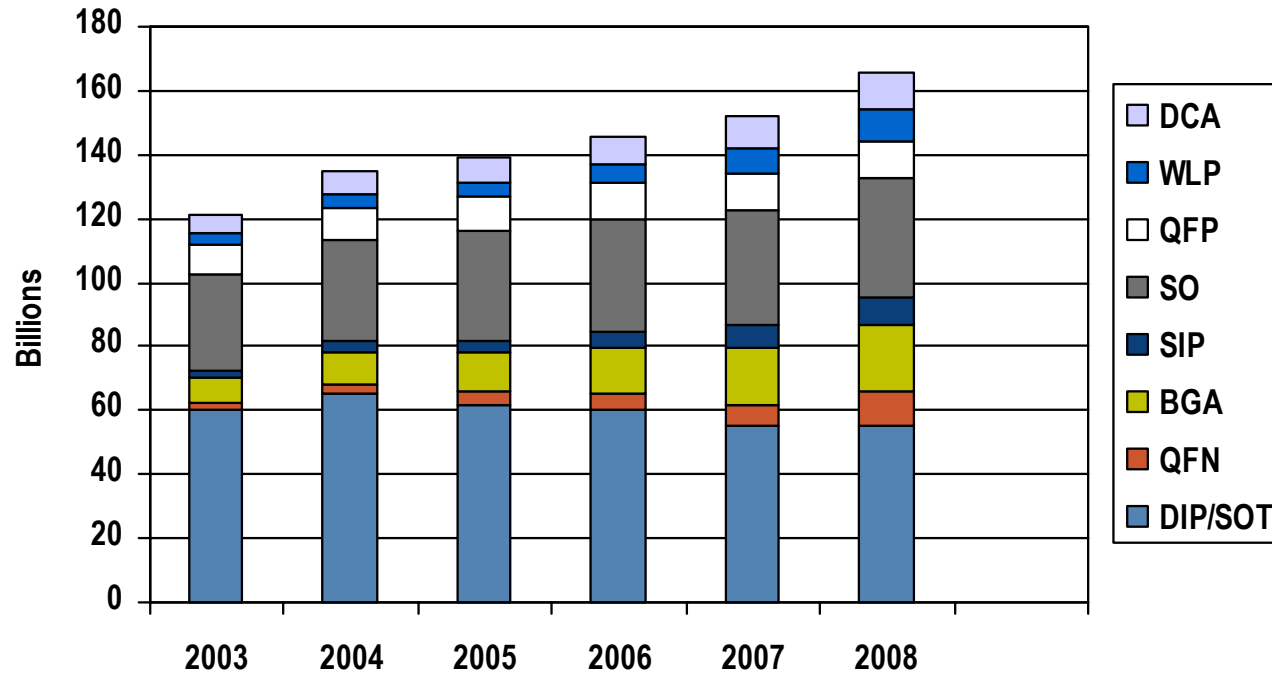
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- **INEMI and ITRS both utilize industry volunteers in working groups to develop a projection on technology requirements over the long term**
- **INEMI tends to focus on system level while ITRS focuses on semiconductor technologies**
- **Given the overlap in packaging INEMI and ITRS cross cut group to coordinate the Packaging Roadmap Chapters.**
- **The 2005 roadmap is just being completed now**
- **If you like to participate in the process please contact me**

- **Volume drivers have shifted to consumer electronics**
- **Longer term growth will be driven by machine to machine**
- **System In Package has become a mainstream technology**
- **Chip Scale Packages are beginning to replace older leadframe technologies due to cost, size, and performance advantages**
- **Wafer level packaging technologies is taking off**
- **The contract assembly and test business has started to consolidate driven by a more competitive environment**
- **The EMS and Assembly and Test overlaps are increasing**
- **Improvements in cost are not keeping pace with pricing pressure**

World Wide Semiconductor Package Volume



Source: Electronic Trends Publications and Prismark

- **Tools and methodologies to address chip and package co-design**
Mixed signal co-design and simulation (SI, Power, EMI)
For transient and localized hot spots - simulation of thermal mechanical stresses, thermal performance and current density in solder bumps
- **Close the Gap between chip and substrate interconnect density**
Increased wireability and dimensional control at low cost
Higher temperature stability and lower moisture absorption
TCE and Modulus better matched to low K flip chip requirements
- **Wafer Level Packaging**
I/O pitch between 250um 400um less than 100 I/O
Solder joint reliability and cleaning processes for low stand-off
Wafer thinning and handling technologies
Compact ESD structures
- **Impact of Cu/low k on Packaging**
Direct wire bond and UBM/bump to Cu to reduce cost
Lower TCE and modulus substrates to reduce die level stress in flip chip
Lower strength in low k which creates a weaker mechanical structure

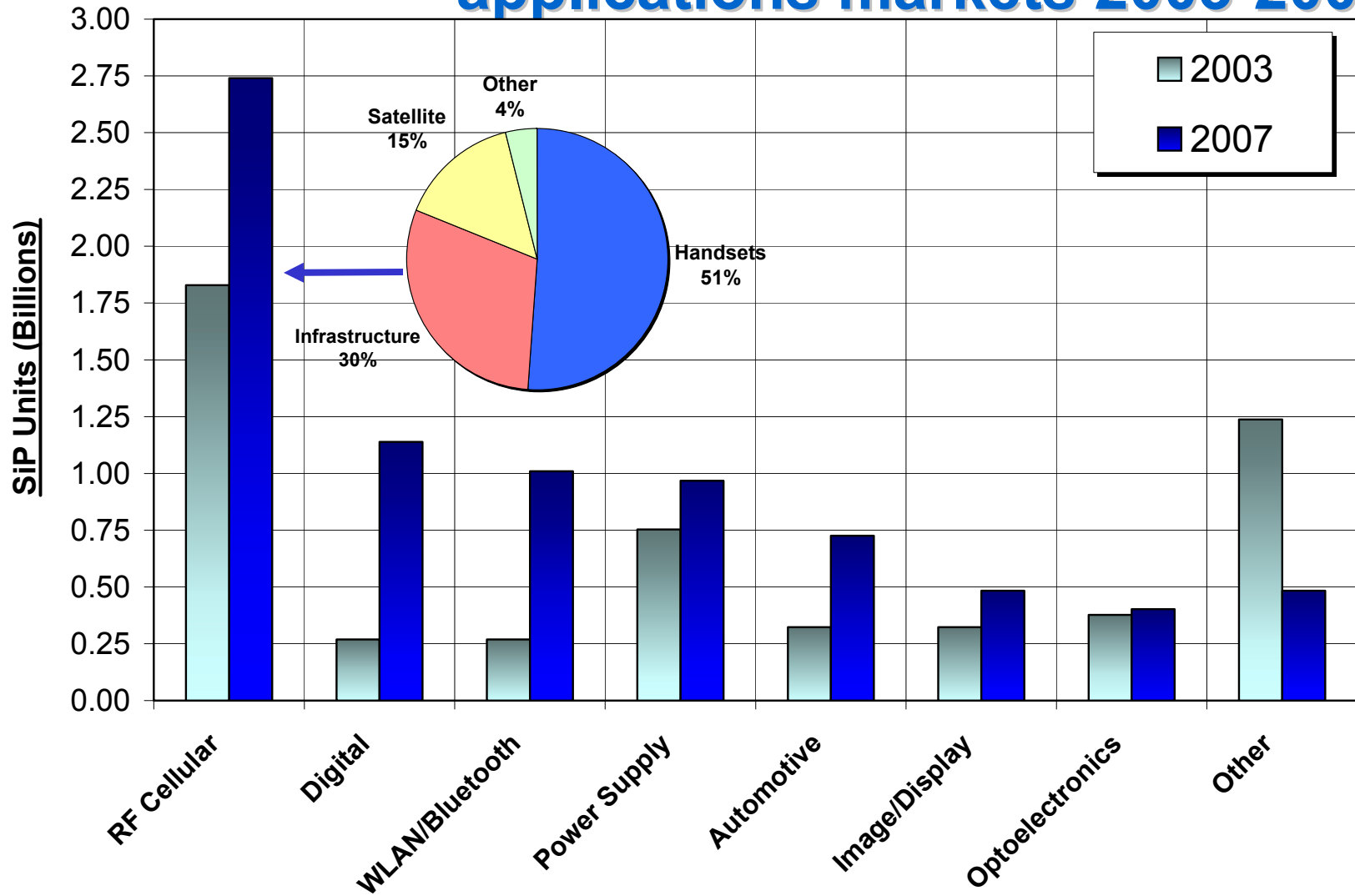
<i>Year of Production</i>	<i>2004</i>	<i>2005</i>	<i>2006</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>
<i>Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)</i>						
Low-cost, hand-held and memory	0.30–.53	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41
Cost-performance	.71–1.24	.67–1.17	.64–1.11	.61–1.05	.58–1.00	.55–.96
High-performance	1.88	1.78	1.69	1.61	1.52	1.45
Harsh	0.32–2.88	0.29–2.60	0.26–2.33	0.25–2.11	0.23–2.00	0.22–1.90
<i>Chip Size (mm²) [3]</i>						
Low-cost	100	100	100	100	100	100
Cost-performance	140	140	140	140	140	140
High-performance	310	310	310	310	310	310
Harsh	100	100	100	100	100	100
<i>Maximum Power (Watts/mm²) [4]</i>						
Low-cost (Watts) [5]	2.7	2.8	3	3	3	3
Cost-performance	0.6	0.65	0.7	0.74	0.79	0.83
High-performance	0.51	0.54	0.58	0.61	0.64	0.64
Harsh	0.16	0.16	0.18	0.18	0.2	0.2
<i>Package Pincount Maximum [6][7]</i>						
Low-cost	122–500	134–550	144–600	160–660	180–720	180–800
Cost-performance	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
High-performance	3000	3400	3800	4000	4400	4600
Harsh	500	550	600	660	720	780

<i>Minimum Overall Package Profile (mm)</i>	<i>2004</i>	<i>2005</i>	<i>2006</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>
Low-cost	0.5	0.5	0.5	0.5	0.5	0.5
Cost-performance	0.8	0.8	0.8	0.8	0.65	0.65
High-performance	N/A	N/A	N/A	N/A	N/A	N/A
Harsh	0.8	0.8	0.8	0.8	0.8	0.8
<i>Performance: On-Chip (MHz)[8]</i>						
Low-cost	552/5200	607/3865	668/4251	735/4676	800/5000	830/5150
Cost-performance	3990	5170	5630	6740	—	—
High-performance	3990	5170	5630	6740	—	—
Harsh	80	88	96	106	116.6	128.26
<i>Performance: Chip-to-Board for Peripheral Buses (MHz) [9]</i>						
Low-cost	100	100	100	100	100	100
Cost-performance (for multi-drop nets)	533	600	667	733	800	800
High-performance (for differential-pair point-to-point nets)	2500	3125	3906	4883	6103	7629
Harsh	80	88	96	106	106	115

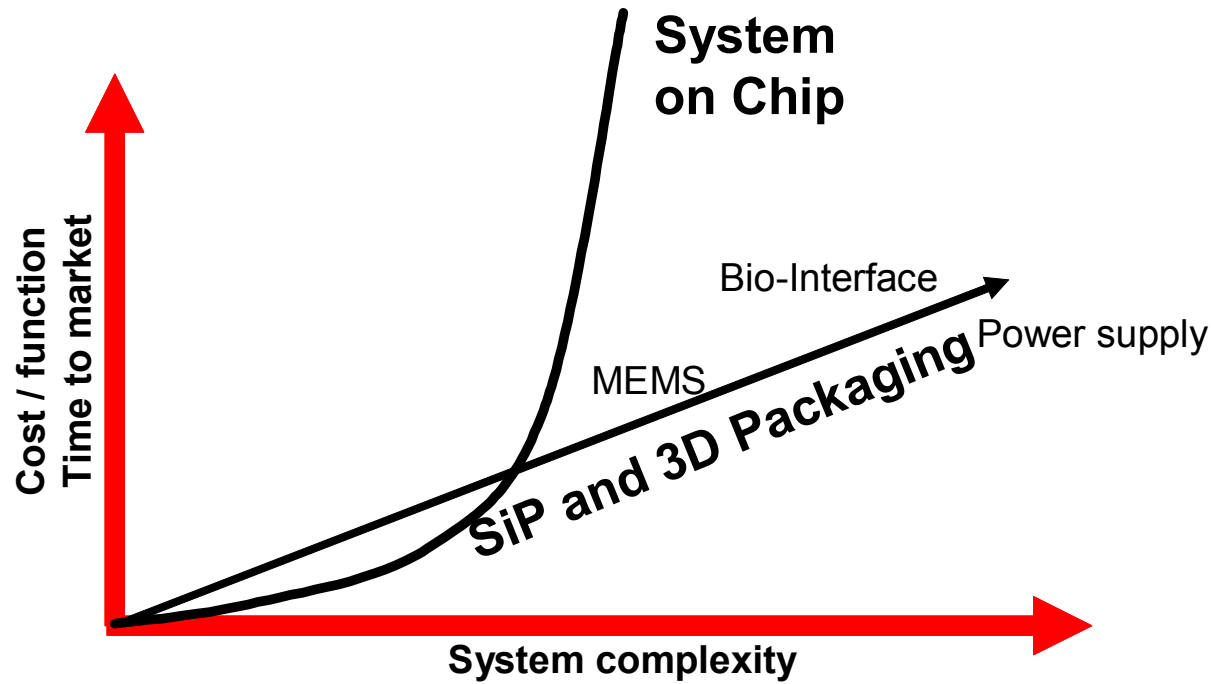
<i>Year of Production</i>	<i>2004</i>	<i>2005</i>	<i>2006</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2012</i>	<i>2013</i>	<i>2015</i>	<i>2016</i>	<i>2018</i>
Wire bond pitch - ball	40	35	35	30	30	25	25	25	25	25	25	25
Wire bond pitch -wedge	30	30	25	20	25	20	20	20	20	20	20	20
TAB	35	30	30	25	25	25	20	20	20	15	15	15
Flip chip area array*	150	130	130	120	110	100	90	90	90	80	80	70
Peripheral flip chip Stud Bump	60	40	40	30	30	20	20	20	20	15	15	15
Note: Validation for 100 um pitch required												

<i>BGA Solder Ball Pitch (mm)</i>	<i>2004</i>	<i>2005</i>	<i>2006</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2012</i>	<i>2013</i>	<i>2015</i>	<i>2016</i>	<i>2018</i>
Low-cost and hand-held	0.8	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
Cost-performance	0.8	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
High-performance	1	1	0.8	0.8	0.8	0.8	0.65	0.65	0.5	0.5	0.5	0.5
Harsh	0.8	0.8	0.8	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5
<i>Chip Scale Package Pitch</i>	0.4	0.3	0.3	0.2	0.2	0.2	0.2	0.15	0.15	0.15	0.1	0.1

Projected growth for SiP in key applications markets 2003-2007



Sources: Prismark .



<i>System In Package Requirements</i>												
<i>Year of Production</i>	<i>2004</i>	<i>2005</i>	<i>2006</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2012</i>	<i>2013</i>	<i>2015</i>	<i>2016</i>	<i>2018</i>
<i>Digital networks- max I/O</i>	<i>2600</i>	<i>2900</i>	<i>3000</i>	<i>3200</i>	<i>3500</i>	<i>3500</i>	<i>3500</i>	<i>3500</i>	<i>3500</i>	<i>3500</i>	<i>3500</i>	<i>3500</i>
<i>RF products - max I/O</i>	<i>150</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>	<i>200</i>
<i>Max number of stack die</i>	<i>6</i>	<i>7</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>	<i>8</i>
<i>Max number die in Module</i>	<i>10</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>	<i>12</i>
<i>Minimum Component size in.</i>	<i>0201</i>	<i>0201</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>	<i>01005</i>
<i>Die Pad pitch - wirebond</i>	<i>40</i>	<i>35</i>	<i>35</i>	<i>30</i>	<i>30</i>	<i>25</i>	<i>25</i>	<i>25</i>	<i>25</i>	<i>25</i>	<i>25</i>	<i>25</i>
<i>Die pad pitch - flipchip</i>	<i>150</i>	<i>130</i>	<i>130</i>	<i>120</i>	<i>110</i>	<i>100</i>	<i>90</i>	<i>90</i>	<i>80</i>	<i>80</i>	<i>70</i>	<i>70</i>
<i>Embedded Passives in Laminate</i>	<i>L</i>	<i>L</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>	<i>CL</i>
<i>Embedded Passives in Ceramic</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>	<i>R, L, C</i>
<i>MSL Level</i>	<i>2a</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>	<i>2</i>
<i>Mx Reflow temp C</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>	<i>260</i>

- **System In Package Thermal Management**
- **Design tools and simulation for new complex 3D structures**
- **Wafer to wafer bonding**
- **Through wafer via structures an via fill process**
- **Bumpless interconnect architecture**

- **System In Package Reliability Projects**

- Thermal mechanical modeling of complex SIP structures and materials combinations**

- Development of passive component test methods for embedded components in mold compounds**

- Analysis of materials properties under reflow conditions**

- Lead free solder joint integrity in embedded SIP applications**

- Solder joint reliability for low stand-off solder joints in**

- Very thin organic film materials properties and adhesion mechanisms in this epoxy bonds**

- Thin die mechanical properties under varying surface conditions**

- Analysis of electroless finish plating solder joints**

- Interfacial resistance of conductive epoxy pastes**

- **SIP Manufacturing Productivity Improvement Projects**
 - Alternative singulation techniques**
 - Mechanical sawing process development**
 - Alternative die attach techniques – electrically & thermally conductive films**
 - Factory Standards**
 - PCB solder mask to mold compound adhesion measurement methods, correlation to CSAM**
- **SIP Substrate and Interconnect Technology Projects**
 - Low cost patterning techniques for interconnect**
 - Drilling processes**
 - High frequency design and simulation tools for RF and mix signal design**
 - Low cost mixing of high frequency with high power dissipation**

- **SIP and 3D technologies will be a key enabler for future electronics growth which are shifting the industries research focus**
- **To improve R&D return and effectiveness the industry needs to increase collaboration through partnerships and shared R&D**
- **Emerging devices will required a new set of packaging technologies that allow devices to interact with the environment instead of being protected from it**

RF System Technology Comparisons



	Stacked IPD HDI Laminate	SMT / Embed Passives on HDI Laminate	Embed Passives on LTCC	SOC
Size	++++	+++	++++	+++++
Design Complexity	+++	++++	+++	+
Development Time	+++	++++	++	+
Development Cost	\$\$\$	\$	\$\$\$	\$\$\$\$
Performance	++++	+++	+++	+++
Technology Availability	+	++++	++	++++
Reliability	++++	++++	+++	++++
Product Cost	\$\$\$	\$\$\$	\$\$\$\$	\$